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Multi-level cell storage with a modulated current method for phase-change memory using Ge-doped SbTe

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A B S T R A C T

We demonstrate a high-speed multi-level cell (MLC) storage for the phase-change memory using a Ge-doped SbTe (GeST) for the first time with a conventional pore-type device structure and a conventional modulated-current writing method. The GeST was selected to have a low Sb-to-Te ratio of 1.8 ($GeST_L$), rendering a diminished growth rate relative to the case of a high Sb-to-Te ratio typically of fast, growth-dominated crystallization. With a writing time of less than 100 ns, each of the 4 resistance levels separated from one another at least by the factor of 4 is shown to form reliably and stay with a low drift coefficient of ~0.1. $GeST_L$ may be regarded as a promising material for high-speed MLC phase-change memory application.

Phase-change memory (PCM), which is based on the reversible phase transition between an amorphous (RESET) state and a crystalline (SET) state of a chalcogenide alloy, has been widely considered as a promising candidate for the next generation non-volatile memory application [1–6]. PCM has RAM-like bit-alterability together with non-volatility, fast read speed, high endurance, good compatibility with standard CMOS fabrication processes and the potential for device scaling beyond the forecasted limits of Flash technology [1–4]. In order to enhance the storage density and reduce the cost-per-bit for PCM at any lithographic technology node, implementation of multi-level cell (MLC) storage has been proposed [4–6]. The MLC storage programs a selected PCM cell to any of n (with $n > 2$) data states (resistance levels), so that each cell in the memory array stores $\log_2 n$ bits of digital information [4]. However, the programmed levels tend to spread due to various processing and environmental disturbances. Thus, the write-and-verify (WAV) scheme is employed to ensure the formation of multiple resistance levels sufficiently close to their respective targeted levels [4–6]. As a rule, repetitive WAV cycles are required to write a single data state properly and this is time-consuming. For example, T. Nirschl et al. reported that it took about 1 μs to complete a WAV cycle for the $Ge_2Sb_2Te_5$ (GST)-based PCM by using a modulated-current (MC) method for writing, and 6–12 WAV cycles *viz.* ~10 μs were needed to write a data bit for over 60% of PCM cells in the memory array [6]. Obviously, a PCM with faster programming/erase (P/E) speed is required to speed up a WAV cycle. In this regard, PCM with a Ge-doped SbTe (GeST) active layer is attractive due to its much faster P/E speed by about one order than that of the GST-based PCM [3]. However, GeSTs with high Sb-to-Te ratios present very fast growth-dominated crystallization [7], which tends to make the MLC storage of GeST-based PCM operated with the existing writing methods practically unfeasible. This seems to account for the lack of demonstration of the sort to date. In our earlier study using GeSTs of varying Sb-to-Te ratios from 4.2 to 1.9, it was shown that the growth rate diminished monotonously with the decreasing Sb-to-Te ratio [7]. In this study, we selected GeST of a low Sb-to-Te ratio of 1.8 ($GeST_L$) with the aim of exploiting the diminished growth rates to form and control multiple resistance levels reliably. With a pore-type PCM device architecture and the MC method, a high-speed 4-level storage for the $GeST_L$-PCM is successfully demonstrated.

The $GeST_L$-PCM devices were fabricated and characterized following essentially the same procedure as in our earlier study [3]. An about 300-nm-thick bottom electrode composed of TiN/Ti was sputter-deposited and patterned by photolithography and wet etching. Contact pores of the size of 150 × 150 nm^2 were formed by electron beam lithography followed by reactive ion etching. After annealing at 350 °C for 30 min in an N_2 ambient, a 300-nm-thick $GeST_L$ ($Ge_{9.8}Sb_{57.9}Te_{32.3}$ in atomic percent) was co-sputtered from a Ge and a SbTe target to fill the contact pore. An about 300-nm-thick TiN/Al top electrode was then deposited *in situ*. For comparison, devices with a $GeST_M$ (Sb-to-Te ratio of 3.06) and $GeST_H$

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(Sb-to-Te ratio of 4.53) were also fabricated following the same procedure. During the PCM device characterization, writing pulses were applied with a pulse generator, and the resulting waveforms were recorded by an oscilloscope having an internal resistance of 50 Ω. The changes in resistance brought about by writing pulses were measured using a source-measure unit (SMU) at the read current of 1 μA. The load resistance of 1 k Ω was used as a current limiter.

Referring to the growth rates of ref. [7] measured during laser-induced crystallization of Ge (5 at.%)STs, the growth rates of $GeST_L$, $GeST_M$ and $GeST_H$ may be taken roughly as ~0.7 m/s, ~3.6 m/s and ~5.9 m/s, respectively. The lowered growth rate of $GeST_L$ is believed to provide a better control of the size of the amorphous region. For example, during the falling time (t_f) of 20 ns of a writing pulse, recrystallization of the supercooled $GeST_L$ tends to be limited to the order of 10 nm or so and the size of the amorphous region can be varied with much control with respect to the contact pore size of 150 × 150 nm^2. As a result, the $GeST_L$-PCM is likely to accomplish multiple resistance levels when either the MC method or the modulated quench (MQ) method is applied [5]. By contrast, the recrystallization of $GeST_M$ and $GeST_H$ is expected to take place extensively on the order of 100 nm under the same condition, which hardly leaves any room for controlling the sizes of the amorphous regions for the MLC storage. In light of the measured growth rates of GeSTs [7], the Sb-to-Te ratio may need to be less than 2.0 (*viz.* a growth rate to be less than ~1.0 m/s) in order to achieve an effective control of the multiple resistance levels for our devices.

Note that the nucleation time of $GeST_L$ (~μs) is much larger than t_f (less than 100 ns) for complete recrystallization of the amorphous region with the size of the contact pore [7]. Thus, it is reasonable to expect that nucleation plays little role in the formation of multiple resistance levels. As a consequence, a percolation-like conduction across the amorphous $GeST_L$ with crystalline inhomogeneties inside is unlikely to occur. Most probably, conduction via the crystalline $GeST_L$ (c -$GeST_L$) around the amorphous $GeST_L$ (a-$GeST_L$) at the contact pore is inevitable, and this results in a programmed resistance of $R_{prog} \propto R_{SET} \times (1 - \frac{S_{prog}}{S_{contact}})^{-1}$, where R_{SET} is the resistance of a PCM cell at the complete crystalline state, and S_{prog} and $S_{contact}$ are the sizes of the amorphous region and the contact pore, respectively, as shown in Fig. 1.

Current-resistance (I-R) characteristics of PCM devices with $GeST_L$, $GeST_M$, and $GeST_H$ are shown in Fig. 2(a). It is found that the $GeST_L$-PCM shows abrupt transitions between the SET and the RESET states when writing pulses with a short t_f, e.g., 5 ns, are applied. With t_f increasing from 5 ns to 20 ns, the transition from the SET state to the RESET state progresses more gradually [8], providing a proper margin for MLC writing with the MC method. For example, a SET state is formed at the resistance of about 10^3 Ω (corresponding to the data level 00) by a current pulse with the waveform of 5/60/5 ns and the amplitude of 2.0 mA. The other data levels of the same PCM are formed at the resistances of about 10^4 Ω, 10^5 Ω and 3 × 10^5 Ω (corresponding to the data levels of 01, 10 and 11, respectively), by current pulses with the waveform of 5/60/20 ns and amplitudes of 2.8 mA, 3.1 mA, and 3.5 mA, respectively. This programming margin (~0.7 mA) is large enough to perform reliable MLC programming even at the array level especially if a WAV scheme is adopted. It is emphasized that such gradual variation of R with I is unachievable for the $GeST_M$- and $GeST_H$-PCMs using the same writing parameters. However, in the case of $GeST_M$-PCM, a slight tendency of gradual RESET is observed, as shown in the circled portion of Fig. 2(a). These results are in a good agreement with our postulate that the growth rate is a determining parameter for the formation of multiple resistance levels.

The programmed resistance levels were readily reproduced throughout 10^3 P/E cycles using the proposed writing parameters for a selected $GeST_L$-PCM cell, as shown in Fig. 2(b). A 4-level storage is thus demonstrated, and its operating speed is significantly faster than that of GST-based MLC storage. For example, it takes about less than 1 μs to store the data state 00 when typically 10 WAV cycles are carried out with the $GeST_L$ MLC, while it takes about 10–35 μs to do the same with the GST-based MLCs [4–6]. It is

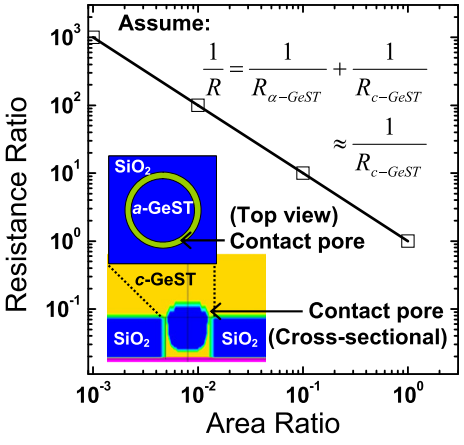

Fig. 1. Correlation between sizes of the amorphous region and the resulting resistance levels estimated from analogy with coaxial parallel resistors. (The area ratio is $1 - S_{prog}/S_{contact}$, and the resistance ratio is R_{prog}/R_{SET}).

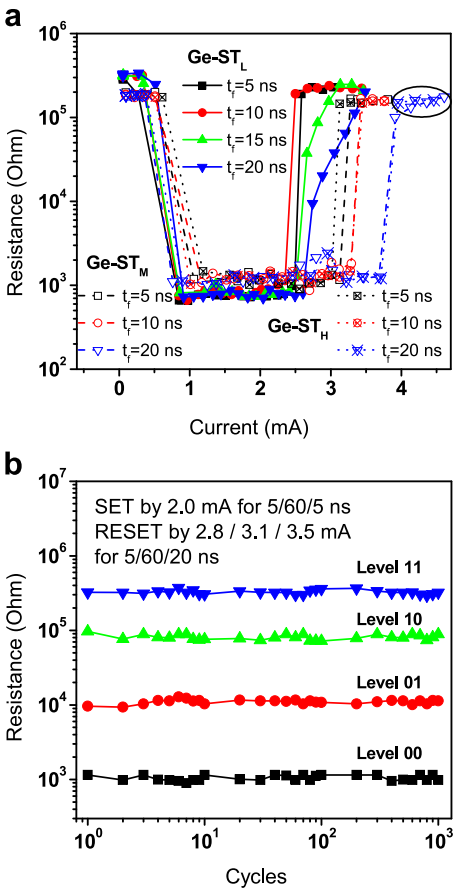

Fig. 2. (a) Current-Resistance characteristics of PCMs using $GeST_L$, $GeST_M$, and $GeST_H$ tested in the temperature of 300 K. (b) Programming/erase cycling endurance of the $GeST_L$-PCM during a 4-level storage.

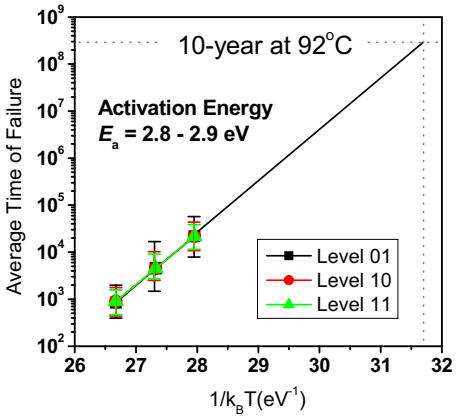

Fig. 3. Time of failure as a function of reverse temperature for the programmed resistance levels. The activation energy (E_a) was found to be 2.8–2.9 eV for all the programmed levels.

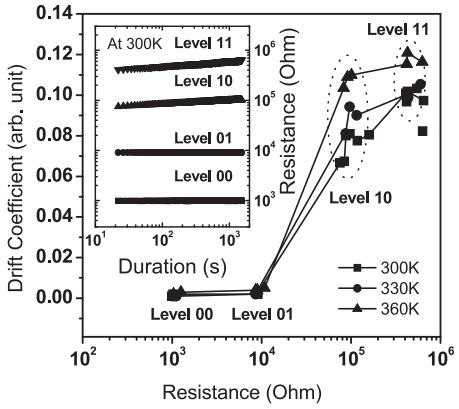

Fig. 4. Drift coefficients at various resistances and ambient temperature for the $GeST_L$-PCM. (Inset) Resistance transients of the programmed levels of a $GeST_L$-PCM during 1.2×10^3 s at 300° K.

worthy noting that an MLC storage has been demonstrated for $GeST_H$-PCM by use of modulation of bias polarity [9]. This technique may be applicable to the $GeST_L$-PCM as well either on its own or in combination with the MC method for an extended MLC capability.

A set of $GeST_L$-PCMs were programmed via the WAV cycles to 4 resistance levels, and the programmed PCMs were annealed in the temperature of 140 °C, 150 °C, and 160 °C to accelerate the retention decay. For each data state programmed to one of the 4 resistance levels, time of failure at each annealing temperature was determined as the time required for half of the programmed cells to undergo a spontaneous change of the data state to 00 data state equivalent to the SET-programmed state. Fig. 3 represents the time of failure as a function of the inverse of temperature. From Fig. 3, it is observed that the activation energy (E_a) values for failure are almost the same for three resistance levels (01, 10, and 11): 2.8–2.9 eV [3]. This seems to indicate that the retention decay takes place by the same mechanism for the three data states, in support of our assumption that the different resistance levels are determined by varying sizes of the amorphous region, rather than by varying degrees of crystallinity in the otherwise amorphous region of a fixed size. Fig. 3 also shows that 10-year retention is expected at 92 °C for all the data states of 11, 10, and 01, suggesting scatter-free, durable data storage by $GeST_L$ MLC at up to a relatively high ambient temperature.

The drift characteristics of the 4 resistance levels were examined at three different ambient temperatures, as shown in Fig. 4. As for the level 00 and 01, virtually no drift was observed regardless of temperature. This is due to (nearly) sheer presence of the crystalline $GeST_L$ phase in the two data states as indicated in Fig. 1 and its temperature-insensitive metallic nature as well [10]. However, the drift coefficients of the levels 10 and 11 are significant (~0.067–0.1) and temperature-sensitive due to larger fractions of the semiconducting amorphous phase, as illustrated in Fig. 1. Nevertheless, the drift coefficients of $GeST_L$ are no larger than those of the GST case [5].

In summary, an MLC storage is demonstrated for $GeST_L$-PCM with the conventional pore-type device structure and the MC writing method. Besides high-speed operation, a 4-level storage with the $GeST_L$-PCM is shown to produce promising characteristics with regard to resistance drift and data retention.

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