Modified write-and-verify scheme for improving the endurance of multi-level cell phase-change memory using Ge-doped SbTe

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\textbf{A B S T R A C T}

In this study, a modified write-and-verify (WAV) scheme is proposed for improving the programming/erasing (P/E) endurance of multi-level cell (MLC) phase-change memory (PCM) using Ge-doped SbTe (GeST). A dual reference data read method is developed to detect the level margin decay during P/E cycling, and a trigger condition is designed to trigger self-repair for the degraded cells before any P/E error for the modified WAV scheme. Experimental results suggest that the modified WAV scheme effectively extends the P/E endurance of PCM using GeST during 4-level P/E by at least 10 times. The modified WAV scheme is expected to improve the endurance of MLC–PCM of system applications.

\section{1. Introduction}

Phase-change memory (PCM) utilizes reversible phase transition between the amorphous/crystalline states of a chalcogenide alloy so as to accomplish a high (RESET)/low (SET) resistance data states. PCM has been widely considered as a promising candidate for the next generation non-volatile memory owing to such attributes as RAM-like bit-alterability, non-volatility, moderately fast Programming(P)/Erasing(E)/read speed, good compatibility with standard CMOS fabrication process, and the potential of device scaling beyond the forecasted limit of Flash technology. Indeed, PCM using Ge\textsubscript{2}Sb\textsubscript{2}Te\textsubscript{5} (GST) phase change material has been commercialized recently and further efforts to improve the performances are being made with promising results. As for higher P/E speed, PCM using a Ge-doped SbTe (GeST) material has shown a high promise [1–4]. To boost the storage density, multi-level cell (MLC) programming schemes have been introduced. An MLC scheme programs a PCM cell to any of \(n\) (with \(n > 2\)) resistance levels so that each cell stores \(\log_2 n\) bits of digital information [5–8]. However, due to limited margin between the multiple resistance levels, P/E endurance of an MLC–PCM may not be as good as that of a single-level cell (SLC) PCM. Moreover, the endurance of an MLC–PCM may also be degraded due to the write-and-verify (WAV) scheme which is required for precisely programming the multiple resistance levels, viz., it may take 6–10 WAV cycles to precisely write a data bit for an MLC–PCM cell [6]. In this regard, enhancement of P/E endurance is required for MLC–PCMs.

In this study, a modified WAV scheme is proposed that can detect the development of the P/E endurance decay of an MLC–PCM cell and self-repair the degradation in an early stage of P/E failure. This modified WAV scheme consists of a dual-reference (DR) read method to detect the decay of MLC level margin in combination with a trigger condition to repair the margin decay using a proper reverse bias stress [9–11]. By testing the modified scheme for MLC–PCM cells with the GeST material, we show that it not only effectively extends the MLC endurance for the tested cells but also prevents data read error or SET stuck failure (SSF) successfully during the WAV and self-repair cycling.

\section{2. Endurance characteristics of MLC–PCM with GeST}

Pore-type PCM cells, each having the pore size of 150 \(\times\) 150 nm\(^2\) and a 300 nm-thick GeST material (Ge\textsubscript{9.8}Sb\textsubscript{57.9}Te\textsubscript{32.3} in atomic percent), were fabricated following the procedure described in [3], and the SET/RESET characteristics of the cells can be referred to [5]. It should be mentioned that the composition of GeST was adjusted from that of a high Sb-to-Te ratio featuring a very fast programming speed so as to accomplish MLC programming with the conventional scheme like the modulated current (MC) method [6]. The PCM cells were programmed and erased by bias pulses from a pulse generator, and the changes in resistance

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brought about by these pulses were measured using a source-measure unit (SMU) at the read current of 1 μA. A load resistance of 1 kΩ was used as a current limiter.

Shown in Fig. 1 are four resistance levels of a PCM cell having the GeST varying with repetitive P/E operations at constant bias pulses (see the open symbols). Forward bias pulses with the amplitude of 3.5 V and the waveform of 5/50/15 ns (leading edge/pulse width/trailing edge) were applied to program the data states 00 and the ones with the respective amplitudes of 3.4 V and 3.0 V and a fixed waveform of 5/50/20 ns were applied to program the data states 01 and 10; herein ‘forward bias’ denotes a bias applied to the top electrode of the PCM cell with its bottom electrode grounded and ‘reverse bias’ is reserved to represent the opposite case. All the programmed data states 00, 01, 10 were erased to form the data state 11 (SET state) by forward pulses with the amplitude of 1.5 V and the waveform of 5/50/5 ns. It is found that the data states 00, 01, 10 start to decay considerably with the elapse of 5 × 104, 6 × 104 and 2 × 104 cycles, respectively. The MLC programming becomes disturbed significantly with the degradation of data states 00, 01 and 10, being finally disabled by the merge of the four resistance levels at the SET state, namely, SSF as shown in Fig. 1. All the programmed data states 00, 01, 10 were erased to the data state 11 (SET state) through solid-state crystallization of the respective amorphous state with the forward pulses of the amplitude of 1.5 V and the waveform of 5/50/5 ns.

As the decay of P/E endurance of an MLC–PCM led to SSF eventually, the mechanism of decay should be expected to be no different from that of SSF. Existing studies on SSF have come to a general agreement that SSF is accompanied by material segregation within the programmed volume. It is understood that the atomic species of differing electron negativities are subjected to differing electrostatic forces for electromigration when an electric field is applied to melt the phase-change alloy during program. As a consequence, the phase-change alloy segregates compositionwise after repetitive P/E cycling [9,10]. Reasonably, the degraded cells may be repaired by means of the reverse material segregation, i.e., via counter material flow under the reverse electric field stress [9–12]. Indeed, it was demonstrated that a PCM device worn out to SSF could be refreshed to function properly like a normal device from repair with reverse bias pulses [9]. From the practical standpoint, however, repairing the PCM cells should be carried out before SSF if it can be done anyway. Otherwise, it may allow miswrite of a data bit that may induce a fatal system error. If the decay of the levels 00, 01 and 10 is detected and repaired in the early stage of development of SSF, the endurance of MLC–PCM can be effectively extended.

3. Results and discussion

For early detection of the level margin decay, we propose to apply the DR data read method. Different from the conventional data read method in which the read current (I_{read}) is compared with a single reference current for a particular level (I_{ref1}), the proposed DR data read method compares I_{read} with a set of two reference currents (I_{ref1}, I_{ref2}) simultaneously for each of the multiple resistance levels during MLC programming, as shown in Fig. 2. At the condition of I_{read} > I_{ref1}, the lower resistance data state (‘1’ for instance) is detected; at the condition of I_{read} < I_{ref2}, the higher resistance data state (‘0’ for instance) is detected. When the level margin decays, the higher resistance data states tend to present lower resistances. As a consequence, I_{read} tends to shift towards that of the lower resistance data state, as shown in Fig. 2. At the condition of I_{ref2} < I_{read} < I_{ref1}, the level margin decay is detected but data read error does not occur since I_{read} < I_{ref1}.

Adopting this DR data read method in the modified WAV scheme, the self-repair of the degraded cells may be triggered when the condition of I_{ref2} < I_{read} < I_{ref1} is maintained after an entire sequence of staircase incremental pulses being applied during writing by MC method. A staircase writing pulse with the largest bias is supposed to provide the highest programmed resistance (the lowest I_{read}) during MC writing. All the proper cells in the memory array are required to reach the condition I_{read} < I_{ref2} before the largest staircase bias is applied for writing. With the degradation of cyclability, some cells fail to present I_{read} < I_{ref2} even when the largest staircase bias is applied. In this manner, the degraded cells are detected and self-repair with reverse bias stress is triggered. As I_{read} < I_{ref1} is maintained in any condition, no data read error will occur. Note that the self-repair of degraded cells is activated only when the trigger condition is reached. In all the rest conditions, the modified WAV scheme works in the same way as the conventional WAV schemes [6–8]. The logic of the modified WAV scheme is shown in Fig. 3.

Listed in Table 1 is a complete set of experimental parameters that we utilized for MLC programming according to the modified WAV scheme: forward pulses for P/E, I_{ref2} and I_{ref1} for detecting the trigger condition, and reverse pulses for repairing the degraded cells. A test of the modified WAV scheme was conducted with a procedure greatly simplified to examine the net effect of DR read method combined with the self-repair scheme: firstly, write-DR read-repair (if needed) was attempted at every 10E4 or 10E5 P/E cycles rather than at each P/E cycle and secondly, a conventional WAV cycling was not implemented to writing a data state. For the test, use was made of the same PCM cells that were previously subjected to P/E cycles to SSF (represented by open symbols in
WAV scheme should be in order. Evidently, the scheme is unusable must be made. A final remark on the limitation of the modified tion and compromise of cycling endurance with operating speed be sacrificed when using the modified WAV scheme. The optimiza- merits system applications. However, the operating speed may applying the modified WAV scheme together with the wear-level- be prevented in the entire process of the modified WAV cycling. By MLC–PCM for system applications as data read error due to SSF can modified WAV scheme shall effectively improve the endurance for modifying technique, MLC–PCM may have enough P/E endurance that be prevented in the entire process of the modified WAV cycling. By ...MLC–PCM during WAV cycling (usually 6–10 cycles to write a data bit). Evidently, the limit of the P/E cyclability for the tested PCM cells by at least 10 times. The modified WAV scheme may effectively improve the endurance for MLC–PCM.

**Operating parameters for the modified WAV scheme.**

<table>
<thead>
<tr>
<th>Data state</th>
<th>Level 00</th>
<th>Level 01</th>
<th>Level 10</th>
<th>Level 11</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write bias (V)</td>
<td>3.5</td>
<td>3.4</td>
<td>3.0</td>
<td>1.5</td>
</tr>
<tr>
<td>Write waveform (ns)</td>
<td>5/50/15</td>
<td>5/50/20</td>
<td>5/50/20</td>
<td>5/50/5</td>
</tr>
<tr>
<td>Targeting resistance (Ω)</td>
<td>2 × 10^4</td>
<td>5 × 10^4</td>
<td>2 × 10^4</td>
<td>2 × 10^3</td>
</tr>
<tr>
<td>Current Iref1 (μA)</td>
<td>12</td>
<td>33</td>
<td>125</td>
<td>–</td>
</tr>
<tr>
<td>Current Iref2 (μA)</td>
<td>10</td>
<td>20</td>
<td>100</td>
<td>–</td>
</tr>
<tr>
<td>Repair bias (V)</td>
<td>–3.5</td>
<td>–3.4</td>
<td>–3.0</td>
<td>–</td>
</tr>
<tr>
<td>Repair waveform (ns)</td>
<td>5/5000/5</td>
<td>5/4000/5</td>
<td>5/3000/5</td>
<td>–</td>
</tr>
</tbody>
</table>

**Fig. 3.** The operating logic of the modified WAV scheme, where i = 1, 2, 3, …

Fig. 1) and then repaired with reverse pulses before initiating the test. The MLC characteristics from the modified WAV scheme are shown in Fig. 1 by the solid symbols in the regime where the two different schemes make a clear difference. It is found that the P/E cyclability of the data states 00, 01 and 10 can be readily extended by at least 10 times even with use of the simplified scheme. We expect that a full operation of the modified WAV scheme would improve MLC endurance to a great degree over a possible degradation from a conventional WAV cycling (usually 6–10 cycles to write a data bit). Evidently, the limit of the P/E endurance may not be extendable indefinitely with repeated self-repairs as a gradual material degradation induced by the P/E cycling would eventually lead to a failure of one sort or another including the RESET-stuck failure in the programmed volume and its surroundings. Note that the present experimental results were obtained manually on the cell level and a wafer-level test is not yet to be conducted.

Compared with the other WAV schemes [6–8], the modified WAV scheme as proposed here is the first attempt to detect and repair the level margin decay for MLC–PCM during WAV cycling. The modified WAV scheme shall effectively improve the endurance for MLC–PCM for system applications as data read error due to SSF can be prevented in the entire process of the modified WAV cycling. By applying the modified WAV scheme together with the wear-leveling technique, MLC–PCM may have enough P/E endurance that merits system applications. However, the operating speed may be sacrificed when using the modified WAV scheme. The optimization and compromise of cycling endurance with operating speed must be made. A final remark on the limitation of the modified WAV scheme should be in order. Evidently, the scheme is unusable for an MLC–PCM with unipolar selection devices such as diodes since self-repair with reverse bias stress is then not possible. This scheme would play a significant role, however, in improving the endurance of an MLC–PCM using bipolar selection devices such as MOSFET or ovonic threshold switching device [13].

**4. Conclusion**

In summary, a modified WAV scheme is proposed to detect and repair the level margin decay for MLC PCM using GeST. The proposed scheme is tested on the cell level, and it extends the P/E cyclability for the tested PCM cells by at least 10 times. The modified WAV scheme may effectively improve the endurance for MLC–PCM.

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**References**


