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A Fermi-Level-Pinning-Free 1D Electrical Contact at the Intrinsic 2D MoS_2–Metal Junction

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Currently 2D crystals are being studied intensively for use in future nanoelectronics, as conventional semiconductor devices face challenges in high power consumption and short channel effects when scaled to the quantum limit. Toward this end, achieving barrier-free contact to 2D semiconductors has emerged as a major roadblock. In conventional contacts to bulk metals, the 2D semiconductor Fermi levels become pinned inside the bandgap, deviating from the ideal Schottky–Mott rule and resulting in significant suppression of carrier transport in the device. Here, MoS_2 polarity control is realized without extrinsic doping by employing a 1D elemental metal contact scheme. The use of high-work-function palladium (Pd) or gold (Au) enables a high-quality p-type dominant contact to intrinsic MoS_2, realizing Fermi level depinning. Field-effect transistors (FETs) with Pd edge contact and Au edge contact show high performance with the highest hole mobility reaching 330 and 432 $cm^2\ V^{-1}\ s^{-1}$ at 300 K, respectively. The ideal Fermi level alignment allows creation of p- and n-type FETs on the same intrinsic MoS_2 flake using Pd and low-work-function molybdenum (Mo) contacts, respectively. This device acts as an efficient inverter, a basic building block for semiconductor integrated circuits, with gain reaching 15 at $V_D = 5$ V.

The electrical performance of semiconductor devices is strongly dependent on the electrical contact between metal electrode and semiconductor,[1] which influences maximum current, on/off ratio, and field-effect transistor (FET) polarity. In conventional metal-oxide semiconductor FETs (MOSFETs), heavy doping[2] is usually applied to source or drain to form Ohmic contacts so as to prepare n- or p-type transistors controlled by channel resistance. By contrast, in a Schottky MOSFET the Schottky barrier height (SBH, ϕ_{SB}) for electrons or holes between metal electrode and semiconductor affects the device polarity.[3] A small SBH to the conduction band edge or the valence band edge and Fermi level within bandgap will give rise to n- or p-type transistors. Ideally, the SBH is determined by the Schottky–Mott rule, which relates the vacuum work function of the metal (ϕ_m) to the semiconductor vacuum electron affinity (χ) or ionization potential ($I_p = \chi + E_g$) for holes,[4,5] where E_g is the bandgap of semiconductor.

Interfacial energy states can cause SBH to deviate from the Schottky–Mott rule,[6,7] through a process known as Fermi level pinning.[7] The intensity of the pinning effect can be quantified by the pinning factor (S), which can be estimated based on the change of SBH as a function of the change of the metal work function. The pinning factor varies from $S = 1$ for no pinning (Schottky limit) to $S = 0$ for complete pinning (Bardeen limit). Strong Fermi level pinning effects are well known in semiconductors: pinning factors of 0.3 for Si, 0.1 for GaAs, and 0.05 for Ge have been measured.[8]

Until now, most reports have described that 2D surface-contact MoS_2 FETs show n-type electrical behavior. The pinning factor of MoS_2 tends to fall in the range 0.11–0.15.[9] Fermi level pinning of MoS_2 is attributed to sulfur vacancies,[10] interface dipoles resulting from charge redistribution, orbital overlap, negative ionization of the outmost S atom complex,[11] intrinsic MoS_2 surface defects during mechanical exfoliation process[12] and gap states induced in the van der Waals gap.[13] In particular, metal–S interactions contribute in several ways to strong Fermi level pinning.[13] To overcome the limitation of MoS_2 as an n-type device and to realize a p-type device, insertion of high-work-function and hole-injecting interlayer MoO_x (6.9 eV)[14] was reported. However, ultrahigh vacuum conditions and high temperatures are needed for MoO_x deposition, and the on-current density of the p-type MoS_2 was low. Ionic gating method was also demonstrated for achieving ambipolar

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conductance MoS_2 FETs. Nevertheless, because of serious electron trapping in ionic liquid and small I_{on}/I_{off} ratio, it limits the possibility of studying MoS_2 quantum physics at low temperature. Recently, formation of van der Waals metal contact with a bottom poly(methyl methacrylate) (PMMA) layer[15] have been demonstrated for achieving high-quality p-type MoS_2. PMMA layer will bring serious surface scattering issue, which also hinders the possibility of studying MoS_2 quantum physics at ultralow temperature. A TiO_2 insertion layer between the MoS_2 and the metal contact has also been investigated, and it can only weakly depin the Fermi level.[16] Pt-MoS_2 contact FETs still show n-type electrical behavior.[16] However, high-quality polarity control without any extrinsic doping through depinning methods was seldom achieved and has not been well studied. Fermi level depinning enables further exploration of intrinsic properties and material physics which were previously hindered by Fermi level pinning.

1D contact to graphene was demonstrated by Wang et al., by evaporating a metal contact to an exposed edge of graphene encapsulated between hexagonal boron nitride flakes.[17] This innovative approach achieves low contact resistance in an architecture that minimizes extrinsic scattering in the channel; however, this architecture has not been proved effective to MoS_2.[18] In many experiments, it is understood that the contacts with MoS_2 comprise a combination of 2D surface and 1D edge contacts. In fact, the formation of pure 1D contact has been found to be very difficult for monolayer or few-layer MoS_2 devices, because the film is atomically thin and therefore its contact area is ultrasmall. Moreover, direct formation of Pd– or Au–MoS_2 1D edge contacts is even more difficult due to the weak adhesion of the high-work-function metals. In previous studies, the Cr adhesion layer was applied between the MoS_2 edge and the high-work-function metals to form a conductive 1D edge contact.[19] Until now, the electrical behavior of pure MoS_2 1D edge contact devices without adhesion metal layers has not been well explored.

It was proposed that one can obtain a very efficient contact with a high capability of electron injection and decrease of the contact resistance through the 1D edge-contact configuration. This theoretical analysis indicates that the 1D edge contact at the metal–MoS_2 interface provides strong orbital overlap and thinner tunnel barriers compared to top contacts.[20]

Here, we demonstrate for the first time that 1D edge contacts are free from the multiple origins of the Fermi level pinning,[10–13] depinning the Fermi level. 1D edge contact devices thus can show both n- and p–type performance governed by the Schottky–Mott rule: the polarity can be simply controlled by applying low- or high-work-function elemental contact in 1D edge contact architectures. Using high-work-function Pd contacts and Au contacts, high two-terminal field effect hole mobility (330 and 432 $cm^2\ V^{-1}\ s^{-1}$) was demonstrated, confirming low-barrier contacts to the MoS_2 valence band. Carrier injection mechanisms using metals (Mo, Ti, Pd, and Au) with different work functions were investigated using temperature-dependent I–V measurements. This result was also used to further fabricate an intrinsic MoS_2 inverter by integrating n- and p-type 1D edge contact MoS_2 FETs together, achieving an inverter gain of 15 under $V_D = 5$ V.

In this study, a series of devices were fabricated with different contact metals: Mo, Ti, Pd, and Au. These metals of low or high work functions were chosen to investigate the Fermi level depinning and polarity control in the context. The electron affinity of the multilayer MoS_2 is ≈4.2 eV, and the bandgap is ≈1.2 eV.[21] The 1D edge contact was formed by applying SF_6/O_2 plasma etching on h-BN–MoS_2 heterostructure, as shown in **Figure 1**. The fabrication process schematics

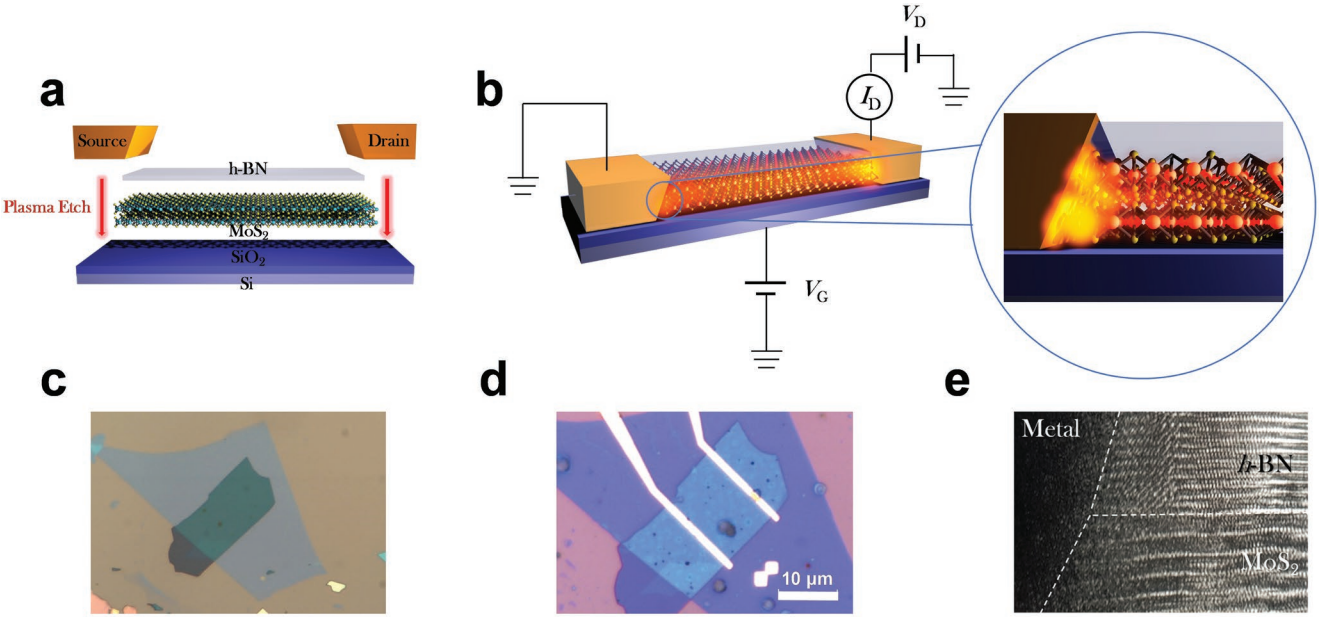

Figure 1. Schematic diagram, optical images, and HR-TEM cross-sectional image of representative MoS_2 1D edge contact FET. a) Schematic diagram shows 1D edge contact FET components. b) Schematic diagram of the 1D edge contact FET circuit with 1D edge schematic details. c) Optical microscopy (OM) image of MoS_2 covered by h-BN. d) OM image of Pd–MoS_2 1D edge contact FET. e) HR-TEM image of Pd–MoS_2 1D edge contact FET contact area.

are shown in Figures S1 and S2 (Supporting Information). Figure 1e shows a high-resolution transmission electron microscopy (HR-TEM) cross-sectional image of the 1D edge contact area, revealing that the metal clearly and firmly contacts with the slanted edge of the multilayer MoS_2 covered by *h*-BN without deformation.

We have performed two-probe measurement on all MoS_2 1D edge contact FETs with the global back-gate configuration mounted on the 285 nm SiO_2 dielectric layer. The quality of the MoS_2 1D edge contact FETs was characterized by performing *I*–*V* measurement at room temperature. **Figure 2** shows the transfer curves and output curves of the Mo–, Ti–, Pd–, and Au–MoS_2 1D edge contact FETs at room temperature. The corresponding gate leakage figures are shown in Figure S3 (Supporting Information), which is negligible compared with on current. All devices with different elemental metal contact show a clear polarity. This metal-dependent polarity is consistent with the Schottky–Mott rule well. Remarkably, both the Pd–MoS_2 and the Au–MoS_2 1D edge contact FETs show very high hole mobility, without extrinsic doping.

Figure 2c,d shows that the Pd–MoS_2 1D edge contact device has a p-type dominant electrical behavior with the hole mobility of 330 $cm^2\ V^{-1}\ s^{-1}$ (*L*: 10 µm, *W*: 16 µm, *T*: 7.5 nm), and the Au–MoS_2 1D edge contact device also shows a p-type dominant electrical behavior with the hole mobility of 432 $cm^2\ V^{-1}\ s^{-1}$ (*L*: 16 µm, *W*: 9 µm, *T*: 82 nm). Here, the two-terminal field-effect mobility was obtained using the linear region model[22] and Equation (S1) in the Supporting Information, as presented in Figure S4 (Supporting Information). In Figure S4 (Supporting Information), we compared MoS_2 1D edge contact FET and conventional double gate FET schematics and equivalent circuits, for extracting accurate field-effect mobility. Photographs and thickness information of the tested devices are presented in S5. All metal electrodes are deposited using an electron beam evaporator deposition system. The deposited metals are polycrystalline films. So, all metal work functions in this research are determined by polycrystalline metals. The Pd work function is ≈5.22 eV,[23] above the multilayer MoS_2 valence band edge. The p-type branch on-current is 6.4×10^{-5} A at $V_G = -80$ V with $V_D = 1$ V. The on/off current ratio is as high as 10^8. The Au work function is ≈5.45 eV,[24] below the multilayer MoS_2 conduction band edge. The p-type branch on-current is 3.3×10^{-5} A at $V_G = -60$ V with $V_D = 1$ V. In the case of Mo and Ti 1D contact FETs, their work functions are ≈4.15 eV[25] and ≈4.33 eV,[26] which are near multilayer MoS_2 conduction band edge. Both Mo and Ti 1D contact FETs show n-type dominant electrical performance. The on-currents of Mo and Ti 1D contact FETs at $V_G = 60$ V with $V_D = 1$ V are 4.8×10^{-6} and 7.6×10^{-6} A, respectively. All samples studied in this research exhibit the similar behavior: the low-work-function metal–MoS_2 1D edge contact devices show n-type dominant electrical behavior and the high-work-function metal–MoS_2 1D edge contact devices show p-type dominant electrical behavior. For a fair comparison, we also compared these results with previous studies on 2D surface contact devices, as shown in Figure 4a. Regardless of the metals applied, all 2D surface contact metal work function position is pinned near MoS_2 conduction band edge, all showing n-type dominant electrical behavior. In the case of 1D edge contact, all metal work function alignment with MoS_2 follows the Schottky–Mott rule very well. And polarity of the devices can be easily tuned only by employing different elemental metal contacts, which clearly indicates the Fermi level depinning from 1D edge contact. Here, we also find the different output curves from p-type dominant Pd- and Au–MoS_2 1D edge contact FETs. Pd–MoS_2 1D edge contact FET shows nonlinear output curve, because of current rectification at Schottky barrier. Schottky emission was found to be the main transport mechanism at subthreshold region by linear fitting as shown in Figure S6 (Supporting Information). Compared with Pd–MoS_2 1D edge contact FET, Au–MoS_2 1D edge contact device shows much linear output curve, owing to smaller SBH

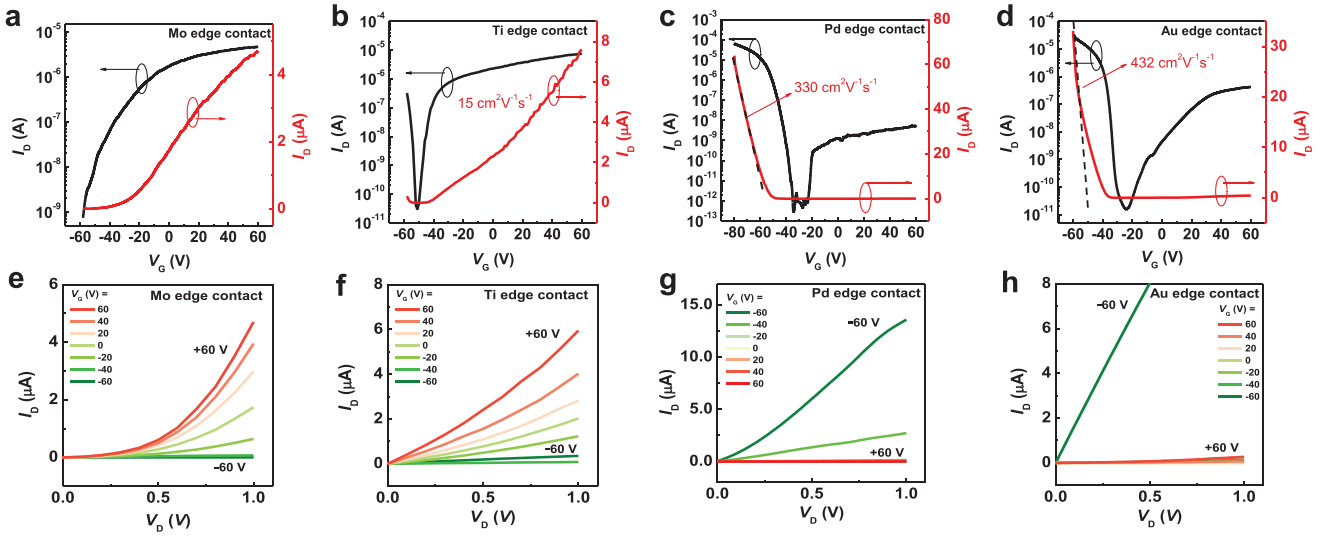

Figure 2. Electrical performance of Mo–, Ti–, Pd–, and Au–MoS_2 1D edge contact FETs. a–d) Transfer curves of Mo–, Ti–, Pd–, and Au–MoS_2 1D edge contact FETs in the log scale (black) and linear scale (red), measured at room temperature. Mo–, Ti–, Pd–, Au–MoS_2 1D edge contact FETs transfer curves were measured at $V_D = 1$ V. e–h) Output curves of Mo–, Ti–, Pd–, and Au–MoS_2 1D edge contact FETs in linear scale, measured at room temperature.

between Au and MoS_2 valence band edge, which allows carrier to be injected from Au into MoS_2 channel much easier.

By now, several methods, including metal work function engineering, chemical doping, electrostatic doping, and ionic gating, have been tested for achieving ambipolar carrier conduction in MoS_2. Extrinsic dopant scattering effect, low conductance buffer layer or electron trapping in ionic liquid at low temperature, rendered to investigate p-type MoS_2 quantum physics at low temperature almost impossible. Here, we performed the electrical measurement on the Pd–MoS_2 1D edge contact device at 9 K using a Cryodyne refrigerator (JANIS CCS-350S). First, we performed the electrical measurement at 273 K, where the same p-type dominant electrical behavior was observed. The hole mobility is 180 $cm^2\ V^{-1}\ s^{-1}$ with the carrier concentration of $2 \times 10^{12}\ cm^{-2}$, as shown in Figure S7a,b (Supporting Information). As we lowered the temperature to 9 K, the device continues to work very well, displaying typical p-type dominant electrical behavior with the carrier concentration of $10^{13}\ cm^{-2}$ and I_{on}/I_{off} of 10^9, as shown in Figure S7c,d (Supporting Information), which indicates standard FET electrical performance from 1D edge contact device at 9 K. The method to calculate field-effect mobility and carrier concentration and analysis of low-temperature electrical performance are shown in Figure S7 in the Supporting Information and addressed through its related explanation. However, it is understood that the surface scattering from the bottom SiO_2 substrate renders a hole mobility to remain at 380 $cm^2\ V^{-1}\ s^{-1}$ at 9 K.

The carrier transport in n- and p-type 1D edge contact FETs was explored by performing temperature-dependent *I*–*V* measurement on Mo–, Ti–, Pd–, and Au–MoS_2 1D edge contact devices, as shown in **Figure 3**a–d. The detailed information of the tested devices is shown in S5. Figure 3 plots the temperature-dependent *I*–*V* measurement results from these devices. All transfer curves are drawn as a function of V_G–V_{TH}, considering the shift in V_{TH} at the different temperatures. Figure 3a,b shows n-type dominant output curves obtained from respective Mo– and Ti–MoS_2 1D edge contact FETs at different temperatures. As Figure 3a,b reveals, the electron current increases with temperature increasing, owing to Schottky emission enhancement. The same measurement was also performed for the Pd– and Au–MoS_2 1D edge contact devices. Figure 3c,d shows p-type dominant temperature dependent transfer curves obtained from the Pd– and Au–MoS_2 1D edge contact FETs. They show the different temperature dependent *I*–*V* measurement results. In Figure 3c, we observe obvious trend of current increase with the temperature increase from Pd 1D contact FET, due to enhancement of Schottky emission which was evidenced by SBH measurement shown in Figure 3g. Figure 3d shows that current doesn't change much corresponding to temperature change with negative SBH as shown in Figure 3h. Moreover, the linear output curve from Au–MoS_2 1D edge contact FET is consistent with negative SBH result from Au 1D contact FET. All these results of n- and p-type MoS_2 are clear indications of Fermi level depinning from 1D edge contact.

For interpreting this result, we measured the SBHs from all these devices. The temperature-dependent transfer curves described above were used to extract the SBHs. In the case of n-type dominant FET, SBH represents the barrier between metal work function position and MoS_2 conduction band edge, while in the case of p-type dominant FET, SBH represents the

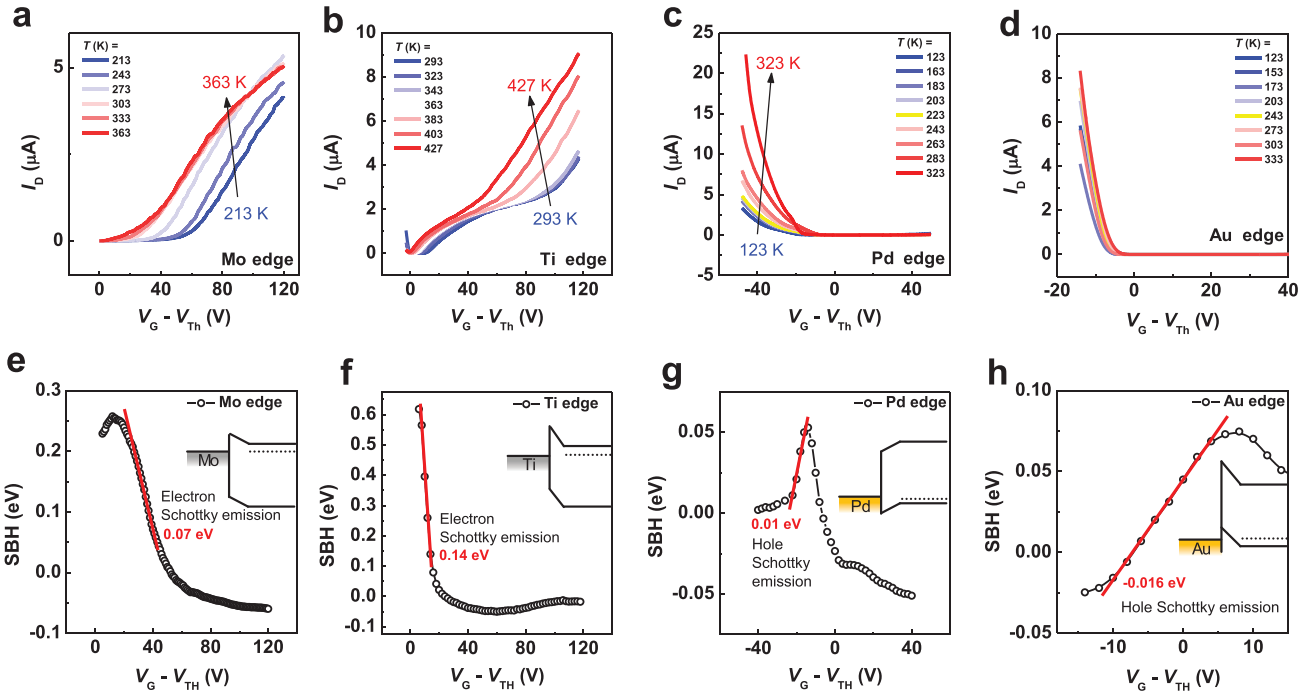

Figure 3. Temperature-dependent *I*–*V* measurement results and SBHs. a–d) Mo–, Ti–, Pd–, and Au–MoS_2 1D edge contact FETs transfer curves were measured at different temperatures, with V_D = 1 V. e–h) Mo–, Ti–, Pd–, and Au–MoS_2 1D edge contact FETs SBHs were plotted as a function of gate voltage. Flat band position SBHs were obtained and marked in the red numbers. Metal–MoS_2 1D edge contact work function alignment is also drawn in (e)–(h).

barrier between metal function position and MoS_2 valence band edge. In Schottky contact devices, the current across the Schottky barrier can be described using the thermionic emission equations,[27] more detailed SBH measurement details are shown in Figure S8 (Supporting Information)

$$I_{2D} = WA^*_{2D}T^2 \exp\left(-\frac{q\varphi_{SB}}{kT}\right)\exp\left(\frac{qV_{2D}}{kT}\right),\ A^*_{2D} = \frac{q\sqrt{8\pi m^* k^3}}{h^2} \quad (1)$$

$$\varphi_{SB} = \frac{k}{q}\left[-\frac{\Delta \ln(I_{2D}/T^2)}{\Delta T^{-1}}\right] \quad (2)$$

Here, W is the channel width, q is the electron charge, k is the Boltzmann constant, A^*_{2D} is the modified Richardson constant, ϕ_{SB} is the Schottky barrier height, V_{2D} is the drain voltage, and m^* is the effective mass. Equation (2), derived from Equation (1), is used to extract the SBH from the negative slope of the linear fit to ln (I_{2D}/T^2) as a function of q/kT.

Under this assumption, the high V_D will reduce the influence of the Schottky barrier at the drain,[9] whereas the current will be mainly determined by the Schottky barrier formed at the source. Here, we applied V_D = 1 V to all devices to obtain the SBH values for a fair comparison. And, all SBHs are extracted from the flat-band position, where thermionic emission is the dominant transport mechanism.

The SBH plots, extracted from temperature-dependent transfer curves in Figure 3a–d from the Mo–, Ti–, Pd–, and Au–MoS_2 1D edge contact devices, are shown in Figure 3e–h, respectively. The SBHs of the Pd- and Au–MoS_2 1D edge contact is found to be ≈10 meV above the valence band edge and ≈16 meV below the valence band edge, respectively, which is consistent with their p-type dominant electrical behavior. The SBHs of the Mo– and Ti–MoS_2 1D edge contact are found to be ≈70 and ≈140 meV, respectively, below the conduction band edge, obeying the Schottky–Mott rule very well, which is also consistent with their n-type dominant electrical behavior. Furthermore, all SBHs from these four different kinds of devices are also consistent with Schottky rectification electrical behavior in Figure S9a–c (Supporting Information), Ohmic transport behavior in Figure S9d (Supporting Information). Here, we compared our results with the previous studies.[9,15] In the previous studies, normal 2D surface contact MoS_2 FETs show n-type electrical behavior. All metal work functions are pinned near MoS_2 conduction band edge. **Figure 4**a shows the metal work function alignment collected from the previous studies on 2D surface contact and this research 1D edge contact. It shows the clear metal work function alignment difference between the 1D edge contact architecture and the 2D surface contact architecture. The pinning factor, based on these 4 different kinds contact metals, is extracted to be 0.975, which is shown in the S10. Figure 4c,h shows the schematic diagram and HR-TEM cross-sectional image of 2D surface contact, while Figure 4d,i of 1D shows those from edge contact. As previously reported, Fermi level pinning of MoS_2 is attributed to sulfur vacancies,[10] interface dipoles resulting from charge redistribution, orbital overlap, Mo—S bonding within the metal–MoS_2 interface, and gap states induced in the van der Waals gap.[13] In particular, metal–S interactions contribute to strong Fermi level pinning[13] in several ways. All these are closely related with metal–MoS_2 interface

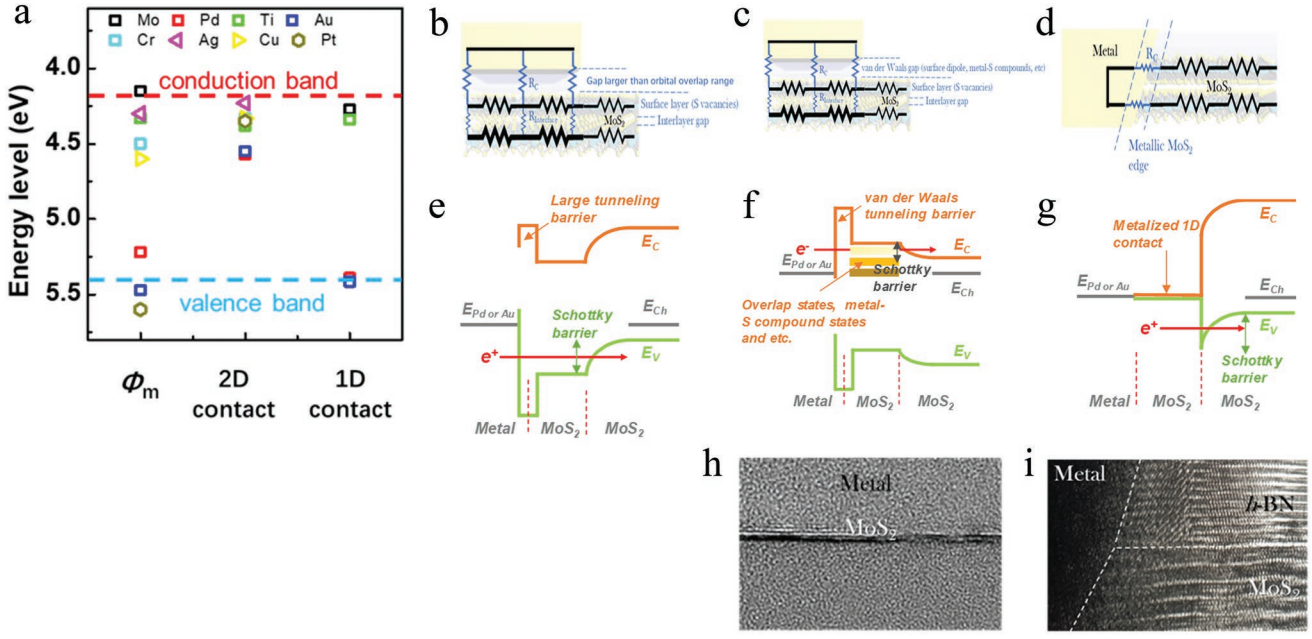

Figure 4. Metal–MoS_2 work function alignment, carrier transport schematics, metal–MoS_2 band alignment and HR-TEM cross-sectional images of 2D surface contact FETs and 1D edge contact FETs. a) Metal–MoS_2 work function alignment based previously studied 2D surface contact FETs and this research 1D edge contact FETs. b,e) Carrier transport schematic and band alignment of MoS_2 2D surface contact with large interface gap (for example, inserting insulating buffer in interface). c,f,h) Carrier transport schematic, band alignment, and HR-TEM contact area cross-sectional image of MoS_2 2D surface contact with van der Waals gap (for example, normal surface contact). d,g,i) Carrier transport schematic, band alignment, and HR-TEM contact area cross-sectional image of MoS_2 1D edge contact with no gap. Contact area was metalized due to metal—MoS_2 strong bond.

topography (2D surface sulfur atom and van der Waals gap size). By now, there are typical three different types of contact schematics that have already been theoretically studied based on different gap sizes, as featured in Figure 4b–d. Different carrier transport mechanisms are shown in Figure 4e–g, respectively. There are van der Waals gap larger than interface orbital overlap range, smaller than interface orbital overlap range, and no van der Waals gap metalized contact conditions. Figure 4b,e presents the condition where the interface gap is larger than metal–MoS_2 orbital interaction range, like inserting insulating buffer layer in the metal-semiconductor interface to avoid the Fermi level pinning from metal semiconductor overlap states.[28] Figure 4c,f represents the condition, like normal metal–MoS_2 2D surface contact, the gap size is within metal–MoS_2 orbital interaction range. Metal orbitals overlap with MoS_2 surface S atoms d-orbital, forming orbital overlap states near MoS_2 conduction band edge, resulting in serious n-type Fermi level pinning.[13] Figure 4d,g shows the metallized contact without a van der Waals gap, where there are no orbital overlap states, avoiding MoS_2 Fermi level pinning. It is achieved using metal–MoS_2 1D edge contact schematic in this research for the first time. Figure 4h,i shows the clearly different interface topographies from 2D and 1D contacts. Compared with 2D surface contact interface, 1D edge contact presents no van der Waals gap between metal and MoS_2, due to dangling bond embedded into metal during electron beam evaporator deposition process, which is also corroborated by 1D edge contact HR-TEM image in Figure 4i. The metal is bounded at the MoS_2 edge with sulfur and molybdenum atoms firmly, forming metalized MoS_2 1D edge contact interface. Comparing parts (h) and (i) in Figure 4, we also find edge contact interface is much cleaner than 2D surface contact interface, with less polymer residue interface states, owing to plasma etching right before metal deposition to 1D edge. It also helps to achieve Fermi level depinning and improve device electrical performance for 1D edge contact.

Inverter is a fundamental building block of digital circuits.[29] A complementary inverter can be fabricated by combining an n-type FET and a p-type FET with a common gate. P-type channel is used as pulling up transistor, while n-type channel is used as pulling down transistor. When V_{IN} is less than the threshold voltage of n-type channel, the n-type channel will be turned off and the p-type channel will be turned on, resulting in equal supply voltage at output. In the case of the V_{IN} larger then threshold, the n-type channel is turned on and p-type channel is turned off, resulting in zero at output. Applying 1D edge contact technic further, we fabricated an MoS_2 inverter without extrinsic doping using a Mo 1D edge contact FET for the n-type component and Pd 1D edge contact FET for the p-type component. For getting better inverter electrical performance, 30 nm thick Al_2O_3 was employed as global back gate dielectric material instead of 285 nm thick SiO_2, because of better carrier concentration tunability. The schematic diagram and the optical image of the inverter are shown in **Figure 5**a,b. The electrical performance of n- and p-type devices were characterized, respectively, as shown in Figure 5c. The electrical performance is measured at n-type component and p-type component threshold exponential overlapping region, which is inverter working region. The inverter electrical performance is shown in Figure 5d. The gain reaches as high as 15 with V_{DD} = 5 V. This result opens a door to realizing complementary integrated circuitry based on high-performance intrinsic MoS_2.

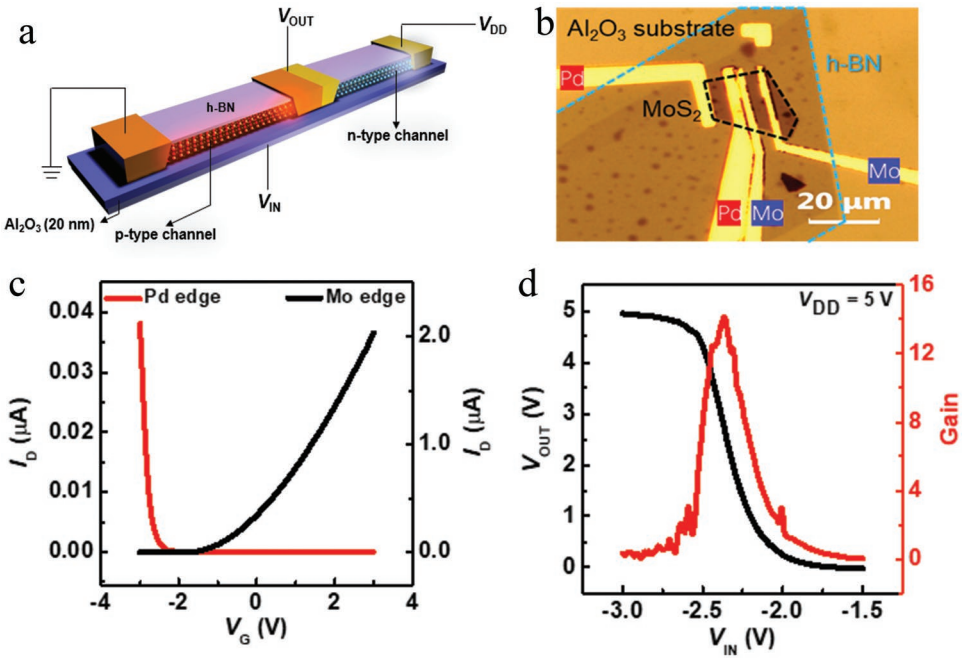

Figure 5. MoS_2 1D edge contact inverter. a) Schematic of MoS_2 1D edge contact inverter. b) Optical image of MoS_2 1D edge contact inverter. c) MoS_2 1D edge contact inverter n-type channel and p-type channel electrical performance. d) MoS_2 1D edge contact inverter electrical performance with gain = 15 at V_D = 5 V.

The origins of the Fermi level pinning were studied theoretically and experimentally. Theoretically, metal–S interactions, orbital overlaps, and states in van der Waals gap are potential origins of Fermi level pinning;[20,30] however, Fermi level pinning of MoS_2, based on the experimental results, is much stronger than the theoretical prediction.[9,15] The atomic vacancies and defects introduced during the device fabrication process appears to enhance the Fermi level pinning effect. Almost all these factors are attributed to the metal–MoS_2 surface interactions, in which the metal is directly evaporated onto the MoS_2 surface. Figure 4c,d shows the different schematic diagrams of the 2D surface contact and the 1D edge contact. For the 2D surface contacted devices, carrier transport takes place from the metal to the MoS_2 outermost S atom surface through the van der Waals gap. All potential Fermi level pinning origins are existing in the van der Waals gap.[10–13] It results in serious Fermi level pinning, when surface contact metals are applied. By contrast, carrier transport in the 1D edge contact takes place directly from the metal to the all-layer MoS_2 edge, without the van der Waals gap. Moreover, the 1D edge contact is clearly gapless compared with the 2D surface contact, without involving van der Waals gap or polymer residues. The top *h*-BN encapsulation layer also prevents damages and contaminations during device fabrication. We also performed the Raman spectra measurement on whole MoS_2/*h*-BN heterostructure before and after plasma treatment, confirming intrinsic MoS_2 quality in the channel. Only 1–2 nm MoS_2 right on the edge are damaged, which are forming a Fermi-level-pinning-free metal–MoS_2 metalized contact. The details are shown in S11, including Raman peak density mapping and Raman peak shift mapping. In the 1D edge contact the physical separation between metal and MoS_2 is much smaller than that of 2D surface contact, which gives rise to the reduction of tunnel barrier widths and the carrier transport loop. Therefore, 1D edge-contact configurations have a higher capability of carrier injection, being free from the origins of Fermi level pinning. Especially, the 1D edge contacts become more significant for metal contacts to multilayer MoS_2 because more edges can be contacted to metals. So, 1D edge contact can simultaneously achieve both Fermi level depinning and high electrical performance. Statistical electrical performance collected from 31 devices is shown in S12, from Mo–, Ti–, Pd–, and Au–MoS_2 1D edge contact devices, where high mobility values are observed clearly. **Table 1** shows the detailed electrical performances of p-type intrinsic MoS_2 FETs in this research and extrinsic doped p-type MoS_2 FETs from previous studies.[14,15,31–39] Compared with previous studies, 1D edge contact FETs show higher hole mobility with high on/off ratio and good stability. In the meantime, quantum transport simulation of Pd–MoS_2 1D edge and 2D surface contact was done for interpreting the mechanism of depinning Fermi level when 1D edge contact is used, as shown in S13. It also shows that Pd work-function position is aligned following Schottky–Mott rule very well in the case of 1D edge contact, as shown in Figure S13a,c (Supporting Information). By contrast, work-function position of Pd is pinned near MoS_2 conduction band edge in the case of 2D surface contact, as shown in Figure S13b,d (Supporting Information), because of the different contact structures resulting in different orbitals overlapping.

Table 1. Comparison of p-type MoS_2 FET electrical performance enabled by different methods. (The data are collected from the devices showing the highest hole mobility in each research. "RT" indicates room temperature in this table. "NA" indicates "not mentioned in the paper.").

Year	Method	Thickness [nm]	$L_{channel}$ [μm]	I_{on} [μA μm^{-1}]	V_D [V]	T [K]	I_{on}/I_{off}	Extrinsic mobility [cm^2 V^{-1} s^{-1}]	Pinning factor	Ref.
2019	Pd 1D contact	7.5	9	3.9	1	RT	10^8	330	0.975	This work
		Multilayer	40	9	1	9	10^8	380		
	Au 1D contact	82	10	3.5	1	RT	10^6	432		
2018	Top InGaZnO film and annealing	49	5.3	0.1	0.1	RT	10^2	24.1	NA (p-type doping)	[37]
2018	Transfer Pt contact and PMMA substrate	Few layer	13.5	8	1	RT	10^6	175	0.96	[15]
2016	$AnCl_3$ doping	8	0.6	21	1	296	10^7	72	NA (p-type doping)	[38]
		10	NA	52 μA	1	133	10^9	132	NA (p-type doping)	
2016	SF_6 plasma doping	21 layers	NA	1.8 pA	2	RT	NA	NA	NA (p-type doping)	[34]
2016	Phosphorus implant doping	20	NA	1.5 μA	3	RT	10^2	137.7	NA (p-type doping)	[35]
2014	Nb doping	Few layer	NA	NA	NA	RT	NA	8.5	NA (p-type doping)	[36]
2014	Pd/MoO_x contact	40	7	1.4	1.5	RT	10^4	NA	NA (p-type contact buffer layer)	[14]
2013	PMMA subatrate	47	NA	230 μS	NA	RT	NA	NA	NA	[32]
2013	SF_6 plasma doping	Few layer	NA	0.08 μA	5	RT	10^2	NA	NA (p-type doping)	[31]
2013	Pd contact	50	2	0.004	0.1	RT	NA	NA	NA	[39]
2012	Ionic gating	15	20	0.4 mS	0.2	220	10^2	86	NA	[33]

In this research, we experimentally demonstrate a new universal approach of Fermi level depinning intrinsic 2D MoS_2–metal junction for the first time, using metalized 1D edge contact. 1D edge contact architecture depins MoS_2 Fermi level and induces recorded high electrical performance p-type intrinsic MoS_2 FETs with room temperature hole mobility of 330 $cm^2 V^{-1} s^{-1}$ (Pd–MoS_2 1D edge contact) and 432 $cm^2 V^{-1} s^{-1}$ (Au–MoS_2 1D edge contact), I_{on}/I_{off} ratio exceeding 10^8 (Au–MoS_2 1D edge contact) and 10^6 (Au–MoS_2 1D edge contact). We also successfully demonstrated MoS_2 CMOS inverter based on the pristine NFET and pristine PFET, using metal–MoS_2 1D edge contact scheme, which also shows recorded high electrical performance. This new depinning architecture is expected to advance the industrialization of MoS_2 nanoelectronics and help study the intrinsic p-type MoS_2 quantum physics at ultralow temperature in the future.

Experimental Section

Fabrication and Measurement of MoS_2 1D Contact FET: Fabrication of the MoS_2 1D edge contact device was started using Scotch-tape to mechanically exfoliate multilayer MoS_2 flakes (purchased from 2D Semiconductors Inc.) onto degenerately doped Si wafer (surface polished and etched, 100 orientation, highly p-type doped, prime silicon wafer purchased from Waferbiz Inc.) covered with 285 nm thick thermally grown SiO_2 serves as global back gate and substrate. The wafer was ultrasonically cleaned in acetone and rinsed in isopropyl alcohol to remove chemical residues before using. Then the *h*-BN was transferred onto MoS_2 by using poly(dimethylsiloxane) (PDMS) dry transfer technique, fully encapsulating MoS_2 flake. A schematic transfer process is shown in Figure S1 (Supporting Information). All transfer process was done below 343 K. With the *h*-BN/MoS_2 heterostructure, a mask was defined by the standard electron beam lithography (EBL) on spin-coated single layer 950 PMMA A6 resist on *h*-BN surface. The electron beam lithography system consists of JEOL JSM-7001F for SEM, Raith EBLPHY Plus and Quantum for lithography. During the EBL, we applied 400 μC cm^{-2} dose and 0.05 μm beam step size. After patterning, we performed controllable plasma etching with a SF_6/O_2 gas mixture using Miniplasma Station from Plasmart. The regions of the flakes outside of the PMMA mask were totally etched away. Only the edge of the MoS_2 was exposed from this multilayer stack structure as the representative device high-resolution transmission electron microscopy cross-sectional image shows (Figure 1e), whose edge is polymer-contaminants-free. HR-TEM cross-sectional image also shows that the 1D edge has the totally different topography from 2D surface. S atoms and Mo atoms are both dangling on the MoS_2 edge having metallic character. The 1D contact schematics are shown in Figure 1b, highlighting the metallic 1D edge. Finally, the metal electrodes (20 nm contact metal covered by 50 nm Au on the top) without any adhesion layer were deposited covering the edges *via* electron beam evaporation at a pressure of 10^{-5} Torr (Korea Vac, KVE-E2000). Schematics of etching and metal deposition processes are shown in Figure S2 (Supporting Information). Note that no further annealing process is needed after metal deposition. All the metals used in this research are purchased from iTASCO (purity, 4N, 99.99%). And 1D cross-sectional of MoS_2 was prepared using focused ion beam technique (JIB-4601F).

Device Measurements: All the electrical measurements were done using the semiconductor parameter analyzer (Agilent 4155C) and the probe machine (MSTECH MST-1000B) with a vacuum level of 10 mTorr. The vacuum chamber is MSTECH M6VC.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

Fermi level depinning, high mobility, intrinsic MoS_2, p-type, transistor

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