Journal of
Nanoscience and Nanotechnology
Vol. 9, 7446–7450, 2009

Dual Phase TiO_xN_y/TiN Charge Trapping Layer for Low-Voltage and High-Speed Flash Memory Application

Gang Zhang and Won Jong Yoo*

Sungkyunkwan University, SKKU Advanced Institute of Nano-Technology, 300 Cheoncheon-dong, Jangan-gu, Suwon, Gyeonggi-do, 440-746, Korea

Flash memory using a dual phase TiO_xN_y/TiN charge trapping layer has been fabricated and its electrical properties were investigated. The TiO_xN_y/TiN layer was formed by partial oxidation of a pre-deposited TiN layer, and the formation of TiO_xN_y/SiO_xN_y was confirmed by high-resolution transmission electron microscopy (HRTEM), X-ray diffraction (XRD), and X-ray photoelectron spectroscopy (XPS) analyses. The enlarged conduction ($\Delta\varphi_c = 3.6$ eV) and valence ($\Delta\varphi_v = 2.5$ eV) band offsets of the TiO_xN_y/TiN to SiO_2 enabled low-voltage (±6 V) and fast programming/erasing (P: 2.7×10^4 V/s and E: -5.1×10^4 V/s) operations, while the transition layer suppressed the trapped charge leakage, giving rise to good 10-year data retention with less than 35% V_{th} decay.

Keywords: Dual Phase TiO_xN_y/TiN, Charge Trapping Layer, Flash Memory.

1. INTRODUCTION

Recently, high-dielectric-permittivity (k) charge trapping layer has been investigated extensively for metal-oxide-nitride-oxide-silicon (MONOS)-type Flash memory application due to the layer's higher trap density and better vertical scalability.[1–4] Meanwhile, it is also possible to meet both the requirements of a small barrier height in the P/E mode and a large barrier height in the retention mode by the work function engineering of the high-k materials in the gate stacks, so as to achieve a faster P/E speed and an extended data retention.[1–4] Therefore, various high-k materials have been proposed for the advanced nano-scaled Flash memory application.[1–6] For example, it has been reported that the P/E speeds of Flash memory with a Hf- or Al-based charge trapping layer were enhanced for the enlarged $\Delta\varphi_c$ or enlarged $\Delta\varphi_v$.[2,3]

Among the high-k trapping materials, it is noted that the dual phase TiO_xN_y/TiN could be a promising candidate for the Flash memory application due to the midgap work function (4.6 eV) [7] of TiN which makes a deeper quantum well ($\Delta\varphi_c$) compared to the electron affinity of Si or Ge. On the other hand, TiO_x has deep $\Delta\varphi_v$ (3.4 eV) to SiO_2.[8] Moreover, TiN belongs to the family of refractory transition metal nitrides, having the physical properties of high melting point, high hardness, and good adhesion to SiO_2 as implied by Gibb's free energy change ($\Delta_f G°$) of formation for Ti–O (−883.2 kJ/mole),[7–10] while the TiO_xN_y-based materials have excellent electrical properties and structural stability to be implemented in the advanced complementary metal oxide semiconductor (CMOS) technology.[10] The dual phase TiO_xN_y/TiN structure is thus expected to retain the advantageous properties of TiN for large $\Delta\varphi_c$ (4.6 eV) and TiO_x for large $\Delta\varphi_v$ (3.4 eV), as well as the superior thermal stability of TiO_xN_y, being a promising candidate for low-voltage and high-speed Flash memory application.

In this work, a dual phase TiO_xN_y/TiN trapping layer was converted from an ultra-thin (~5 nm) pre-deposited TiN film on SiO_2 by partial oxidation. The HRTEM and XRD analyses confirm the existence of un-oxidized crystalline TiN, while the XPS analysis suggests the formation of TiO_xN_y from the Ti–N and Ti–O spectra. A SiO_xN_y transition layer is also detected by XPS from the Si–N spectra. MONOS-type Flash memory with the dual phase TiO_xN_y/TiN trapping layer was fabricated, and excellent capability of low-voltage operation (±6 V) and fast P/E speeds (P: 2.7×10^4 V/s and E: -5.1×10^4 V/s) by using Fowler-Nordheim (F-N) method are observed from the memory devices. Good endurance ($>10^5$ P/E cycles) and data retention (<35% 10-years V_{th} degradation) properties are also demonstrated.

2. EXPERIMENTAL DETAILS

A 3-nm-thick tunnel oxide (SiO_2) was first thermally grown at 875 °C on a p-type ⟨100⟩ silicon wafer. Subsequently, a 5-nm-thick TiN layer was deposited on SiO_2

*Author to whom correspondence should be addressed.

1533-4880/2009/9/7446/005 doi:10.1166/jnn.2009.1775

by e-beam evaporation using a TiN target at 850 °C. The TiN layer was then capped with a 9-nm-thick block oxide formed by low-pressure chemical vapor deposition (LPCVD). Thicknesses of the layers were estimated by an elliposometer. Unlike in the other work,[10] the TiN was oxidized during rapid thermal process (RTP) at O_2 ambient, TiN was annealed at vacuum in this work. Partial oxidation occurred between TiN and SiO_2, and the reaction, $TiN + O \rightarrow TiO_xN_y$, was thermodynamically favorable as indicated by its Gibb's free energy change $\Delta_f G^o = -581.9$ kJ/mole.[11]

The dual phase properties of the TiO_xN_y/TiN embedded in SiO_2 were investigated by the HRTEM and XRD analyses. The cross-sectional TEM image (inset) suggests that the dark grains with lattice fringes (indicated by circles) have the crystalline phases embedded in an amorphous matrix, as shown in Figure 1. XRD analysis was performed on the TiO_xN_y/TiN stacked structure, and it was found that the major peaks were detected at $2\theta = 36°$, 42°, 63.5°, 76.5° which originate from the diffractions from the (111), (200), (220) and (311) planes of TiN, as shown in Figure 1. This result indicates the existence of the unoxidized TiN crystals. The orientation [200] of TiN is preferred. It is understood that TiN is highly textured along the [100] growth direction of Si, from which the (200) peak intensity is stronger compared with the other peaks. The overall energy of the film, which is supplied during deposition, is the summation of the strain energy and the surface energy. The surface energy is 4.0×10^{-4} J cm^{-2} for (111), 2.6×10^{-4} J cm^{-2} for (110) and 2.3×10^{-4} J cm^{-2} for (100).[12] That is, the lowest surface energy plane is (200), while lowest strain energy plane is (111). In this experiment, the remaining TiN aligns in the [200] preferred orientation on the lowest surface energy plane.

In order to investigate the chemical properties of materials in the TiO_xN_y/TiN stack, XPS surface profiling for Ti 2p, N 1s, O 1s, and Si 2p peaks was performed, as shown in Figure 2. The Ti 2p spectra are characterized by the doublets of Ti $2p_{1/2}$ and Ti $2p_{3/2}$, resulting from spin-orbit coupling. Considering that the integrated intensity of the Ti $2p_{1/2}$ peak relative to that of the Ti $2p_{3/2}$ peak is equal to the spin-orbit multiplicity of 0.5 and the spin-orbit splitting is assumed to be ~5.9 eV for all of the states, we can deconvolute the Ti 2p spectra into Ti–N and Ti–N–O bonds. The deconvoluted results of Ti 2p spectra are shown in Figure 2(A), where the Ti $2p_{3/2}$ peaks are observed at 455.6 eV and 456.5 eV due to Ti–N and Ti–N–O bonds that correspond to TiN and TiN_xO_y, respectively. This can be attributed to the chemical reaction between the TiN layer and the SiO_2 layer due to the low free energy change of oxidation for Ti–O or attributed to the oxygen traps of TiN due to the availability of dangling bonds at the TiN/SiO_2 interfaces.[13] Note that the XRD spectra for the TiN_xO_y/TiN in this work are distinct from those for the fully-oxidized TiO_xN_y in which the TiN peaks are negligible,[10] while the XPS spectra for the TiN_xO_y/TiN are different from those for the TiN nanocrystals embedded in Al_2O_3 formed by co-sputtering, in which the peaks for Ti–O are negligible.[14] Based on the results of XRD, TEM and XPS, it is considered that the dual phase TiN_xO_y/TiN has been formed, and the ratio of TiO_xN_y in the dual phase TiO_xN_y/TiN is ~45% according to the amplitudes of the Ti–N–O and Ti–N XPS spectra. In addition, the dual phase TiN_xO_y/TiN trapping layer differs from the TiN nanocrystals trapping sites, as the TiN nanocrystals are mixed with a charge trapping TiO_xN_y matrix for the dual phase TiN_xO_y/TiN, while they are embedded in a dielectric, e.g., Al_2O_3, matrix for the TiN nanocrystals trapping sites.[14]

According to the deconvolution results for Si 2p spectra in Figure 2(B), the peaks at binding energies of 103.1 eV, 102.1 eV, and 98.8 eV for the binding states of Si–O, Si–O–N and Si–Si can be obtained. The deconvoluted O 1s spectra in Figure 2(C) indicate the presence of O–Si (532.6 eV), O–Ti–N (530.7 eV) and O–Ti (529.7 eV) peaks that originate from SiO_2, TiO_xN_y and TiO_2, respectively. The major peaks in N 1s spectra (396.1 eV for N–Ti bond and 397.2 eV for N–Ti–O bond) are attributed to TiN and TiN_xO_y, respectively, as shown in Figure 2(D). In addition, the N–Si–O bonds at 399.3 eV are also detected. The result for the N–Si–O bonds is also consistent with that for the Si 2p spectra in Figure 2(B), and this confirms the presence of SiO_xN_y transistion layer at the interface of the SiO_2 and TiO_xN_y/TiN. This transition layer may be beneficial to the memory window and P/E speed, as it is expected that the barrier height of tunnel oxide is reduced during the P/E operations.[3] The barrier height of the block oxide might also be reduced due to the thermally formed transition layer between TiO_xN_y/TiN and block oxide, but the decrease of programming speed may be negligible since the thickness of the block oxide is much larger than

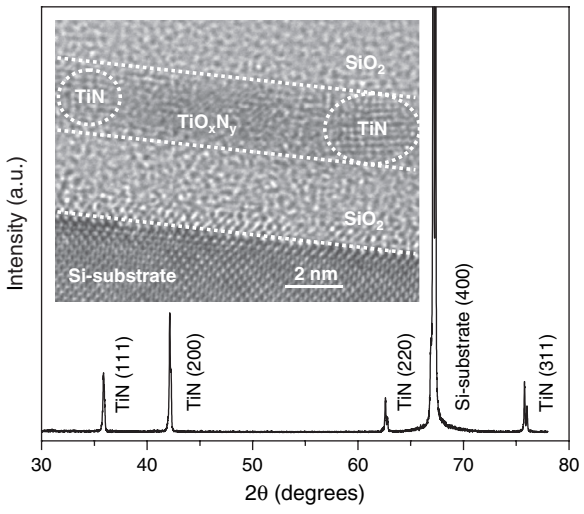

Fig. 1. XRD spectra of the TiO_xN_y/TiN stack embedded in SiO_2. (Inset) The cross-sectional TEM image of the TiO_xN_y/TiN stack.

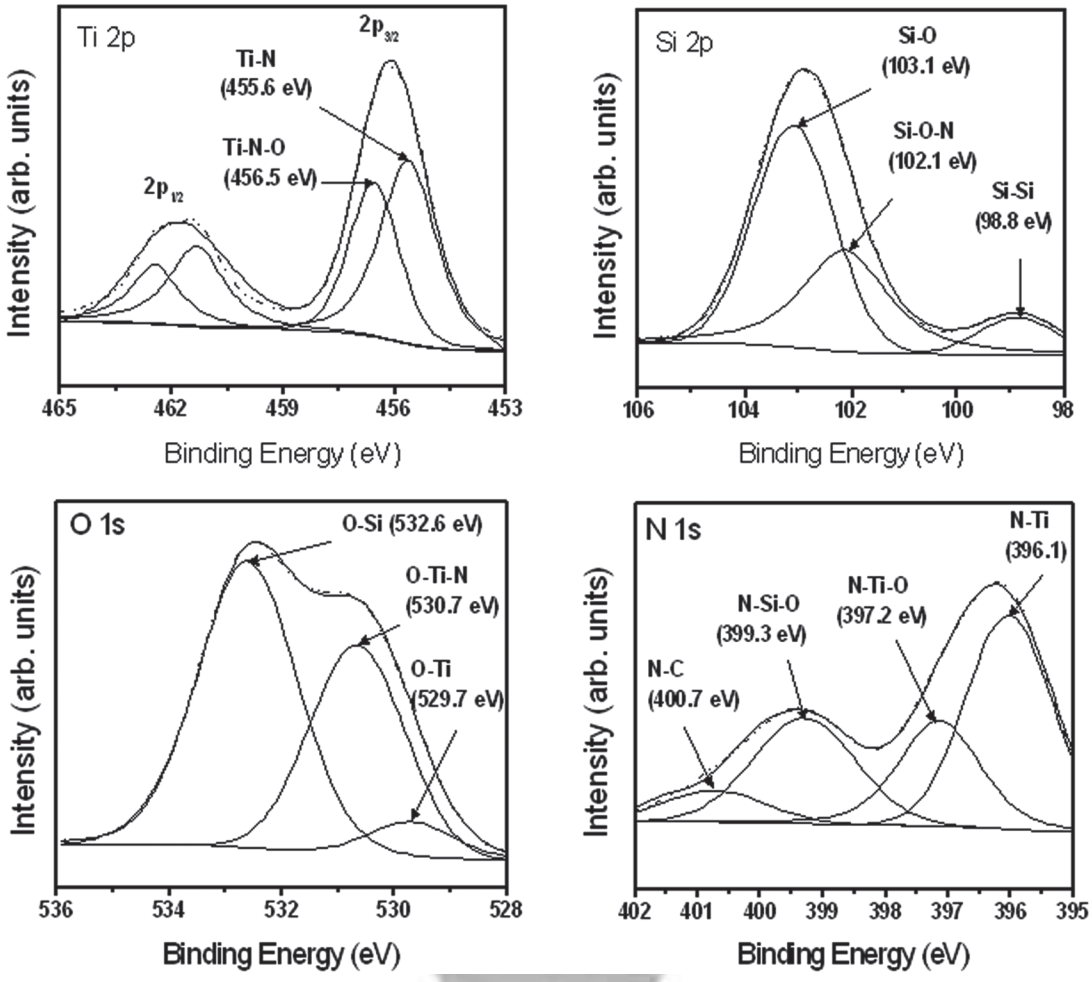

Fig. 2. XPS spectra showing (A) Ti 2p, (B) Si 2p, (C) O 1s and (D) N 1s. Deconvolution results confirm the formation of TiO_xN_y and SiO_xN_y.

that of the tunnel oxide. As a result, the improvement of P/E speed is anticipated for the TiO_xN_y/TiN device.

Based on the proposed method for the dual phase TiO_xN_y/TiN formation, n-MOSFET devices with the $TaN/SiO_2/(TiO_xN_y/TiN)/SiO_2$/p-Si stacked structure were fabricated to demonstrate the memory performances. The device structure is shown in Figure 3(A). The TaN layer was deposited by sputtering using a Ta target in an $Ar+N_2$ ambient, and patterned as a gate electrode, followed by ion implantation (As^+, 1×10^{15} cm^{-2}, 70 keV), RTP activation annealing at 950 °C for 30 s to form the source/drain regions, and forming gas annealing at 400 °C. A possible flat band diagram is drawn by taking into consideration of the transition layer,[8, 10, 15] as shown in Figure 3(B). A control device was fabricated under the same process condition without the TiN layer to confirm the memory effects of the TiO_xN_y/TiN trapping layer.

3. RESULTS AND DISCUSSION

The P/E properties of the 100 μm/10 μm devices with and without TiN using the F-N method are shown in Figure 4 for various applied voltages (0 to ±12 V) and pulse durations (10^{-6} to 1 s). The threshold voltage (V_{th}) changes are enlarged with increasing P/E voltages in the TiO_xN_y/TiN based devices, as shown in Figure 4(A). In contrast, without TiN, no V_{th} shift is observed in n-MOSFET devices in the entire range of the applied P/E voltage. Therefore, it is clearly proven that the TiO_xN_y/TiN is the charge trapping media in the memory device. The V_{th} transient characteristics of the memory device are shown in Figure 4(B), with a V_{th} window of 2.6 V from the P/E voltage of ±12 V. The programming speed determined by dV_{th}/dt, is found to be about $\sim2.7\times10^4$ V/s for all the programming voltages. However, the starting point to attain the maximum speed is clearly observed at ~1 ms for programming voltages of 7–9 V, while it is at ~1 μs for programming voltages of ≥10 V. Saturation starts between 10 ms–100 ms for the programming voltage range of 10 V–12 V, suggesting that the charge tunneling mechanisms are different between the low- and high-voltage operations.

According to the models proposed for the P/E dynamics in the Flash memory devices using a high-k trapping layer,[2, 3] the F-N tunneling via both tunnel oxide and

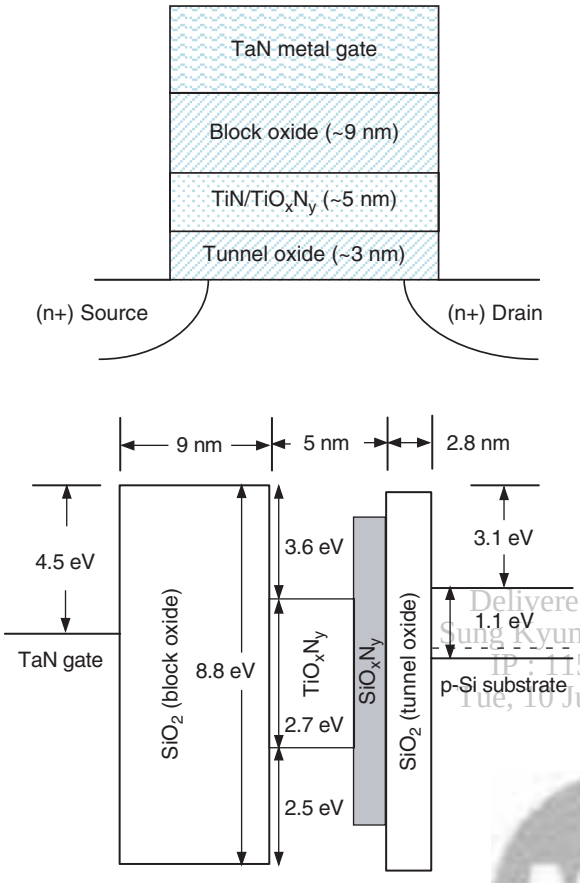

Fig. 3. (A) Schematic of the device structure, and (B) energy band diagram at flat band condition of n-MOS transistor memory device with TiO_xN_y/TiN embedded in SiO_2.

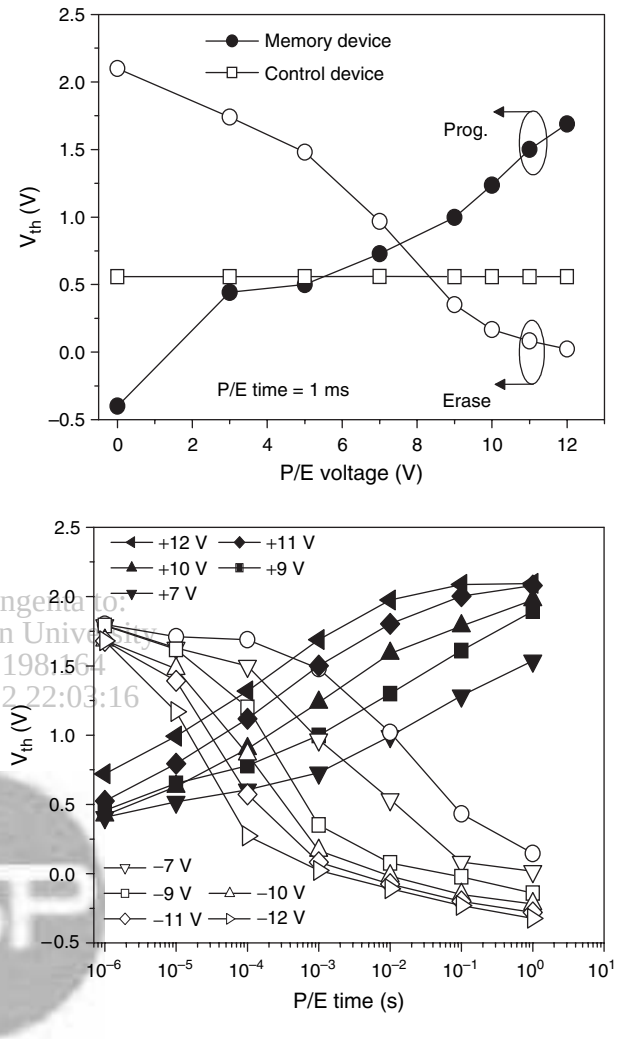

Fig. 4. (A) The V_{th} shift of the TiO_xN_y/TiN memory device as a function of P/E voltages for 1 ms, compared with the control device. (B) V_{th} transient characteristics during P/E operations.

block oxide is the main mechanism for programming at high voltage, and this is similar to the observation in this work. However, a large saturated V_{th} is obtained from high-voltage programming in our experiment. This is due to the deeper energy level resulting from the higher work function of TiN and the electron trapping at the SiO_xN_y transition layer enhanced electron tunneling.[2, 3] Also, in the TiO_xN_y/TiN device the tunneling probability to gate via block oxide is low and in turn more charges can be retained. This requires a higher electric potential of TiN to reach the saturation. According to the reported model,[16] the charging mechanism can be interpreted by F-N tunneling via tunnel oxide and block oxide at low programming voltage ($\leq$9 V). The electric field in the block oxide calculated for gate voltages of 7–9 V is in the range of 5.9–7.6 MV/cm. As the electric field in this range is large (the onset for F-N tunneling is $\sim$6 MV/cm^3), the F-N tunneling of the carriers through the gate stack is expected to be the mechanism responsible for charging at low programming field. However, injection current through tunnel oxide can be induced due to direct tunneling at higher P/E voltages, similar to the reported model.[16] This explains the different programming performances of the memory device at low/high P/E voltages. It is also assumed that reverse-tunneling of the trapped electrons via the tunnel oxide to the substrate is suppressed by the transition layer, which gives rise to enhanced data retention.

The erasing speed is determined by the same mechanisms understood for programming. The erasing speeds are found to be -3.6×10^4 V/s, -4.4×10^4 V/s, and -5.1×10^4 V/s at -7 V, -9 V, and -12 V, respectively. The trends to reach the maximum erasing speed are similar to those of programming at $\sim$10 μs. This indicates that the same tunneling mechanism is responsible for both P/E. Electron tunneling via the tunnel oxide may also occur by the combination of trap-assisted tunneling and direct tunneling, although this has not been proven yet.

The endurance property of the memory device indicates the ability of TiO_xN_y/TiN to capture and release electrons easily without significant degradation of the V_{th} window, even after 10^5 cycles of P/E operation, as shown in Figure 5(A). With a higher P/E voltage ($\pm$12 V for 1 ms), the endurance performance is better up to 10^5 P/E

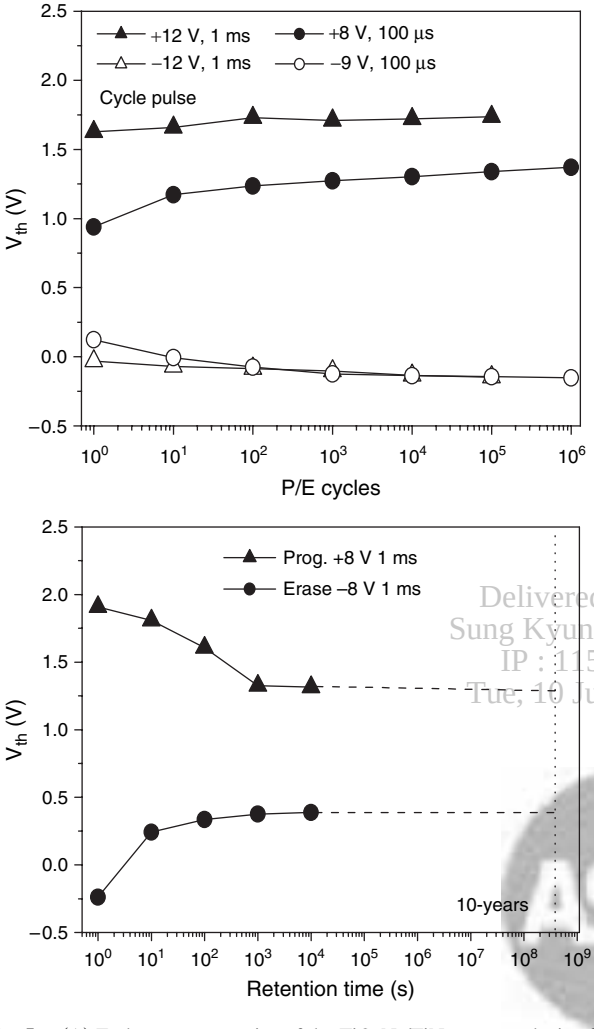

Fig. 5. (A) Endurance properties of the TiO_xN_y/TiN memory device for low- and high-voltage P/E conditions. (B) Retention properties of the memory device at room temperature.

cycles compared to that at lower voltages (+8/−9 V). This indicates that the quality of the tunnel and block oxides is good to endure the stresses. At low-voltage P/E pulses (+8/−9 V for 100 μs), a slight enlargement in V_{th} window is observed, followed by a negligible change. The slower and reversible electron transition from the tunneling levels down to the trap levels in the SiO_xN_y transition layer during the initial operation cycles may be responsible for the change in V_{th}. The data retention characteristics of the memory device are demonstrated in Figure 5(B). The P/E operations are preformed by ±8 V for 1 ms. The V_{th} decay is fast and V_{th} becomes saturated at 10^3 s. Interfacial charge decay from shallow trap levels of the SiO_xN_y transition layer may be faster. It is expected that the V_{th} decay can be suppressed by optimizing the tunnel oxide and the transition layer thickness. After 10^3 s, good retention property is observed due to the deep potential well of TiN.

4. CONCLUSIONS

The Flash memory with a dual phase TiO_xN_y/TiN trapping layer was fabricated by partial oxidation of ultra-thin TiN film which is pre-deposited on a SiO_2 oxide followed by vacuum annealing. HRTEM, XRD, and XPS analyses confirm the formation of the dual phase TiO_xN_y/TiN, which exhibits the electrical properties of both TiN and TiO_xN_y. Significant enhancements in P/E speeds are achieved from enlarged conduction and valence band offsets of the TiO_xN_y/TiN when F-N tunneling is predominant. Good 10-year retention and endurance properties are also demonstrated.

References and Notes

1. T. Sugizaki, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, *VLSI Tech. Dig.* 27 **(2003)**.
2. Y. N. Tan, W. K. Chim, W. K. Choi, M. S. Joo, T. H. Ng, and B. J. Cho, *IEDM Tech. Dig.* 889 **(2004)**.
3. Y. Q. Wang, P. K. Singh, W. J. Yoo, Y. C. Yeo, G. Samudra, A. Chin, W. S. Hwang, J. H. Chen, S. J. Wang, and D. L. Kwang, *IEDM Tech. Dig.* 169 **(2005)**.
4. G. Zhang, W. S. Hwang, S. M. Bobade, S. H. Lee, B. J. Cho, and W. J. Yoo, *IEDM Tech. Dig*. 83 **(2007)**.
5. T. H. Nam, C. A. Yu, J. M. Nam, H. G. Kim, and Y. W. Kim, *J. Nanosci. Nanotechnol.* 8, 722 **(2008)**.
6. G. B. Cho, Y. H. Kim, H. S. Kim, J. Y. Choi, J. M. Lee, and T. H. Nam, *J. Nanosci. Nanotechnol.* 8, 949 **(2008)**.
7. D. R. Lide and H. P. R. Frederiks, CRC Handbook of Chemistry and Physics, 78th edn., Taylor and Francis Group, LLC, London, UK **(1997)**.
8. G. D. Wilk, R. M. Wallace, and J. M. Anthony, *J. Appl. Phys*. 89, 5243 **(2001)**.
9. J. Kim, H. Hong, S. Ghosh, K. Y. Oh, and C. Lee, *Jpn. J. Appl. Phys.* 42, 1375 **(2003)**.
10. S. Choi, S. Jeon, M. Cho, and H. Hwang, *Jpn. J. Appl. Phys*. 42, L102 **(2003)**.
11. M. Wittmer, J. Noser, and H. Melchior, *J. Appl. Phys*. 52, 6659 **(1981)**.
12. J. Pelleg, L. Z. Zevin, S. Lungo, and N. Croitoru, *Thin Solid Films* 197, 117 **(1991)**.
13. H. Sumi, H. Inoue, M. Taguchi, Y. Sugano, H. Masuya, N. Ito, S. Kishida, and H. Tokutaka, *Jpn. J. Appl. Phys*. 36, 595 **(1997)**.
14. S. Choi, S. S. Kim, M. Chang, H. Hwang, S. Jeon, and C. Kim, *Appl. Phys. Lett.* 86, 123110 **(2005)**.
15. C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, *IEDM Tech. Dig*. 613 **(2003)**.
16. C. M. Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita, C. Gerardi, L. Perniola, B. D. Salvo, and S. Lombardo, *IEDM Tech. Dig.* 549 **(2003)**.

Received: 25 February 2009. Accepted: 4 March 2009.