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Fermi-Level Pinning Free High-Performance 2D CMOS Inverter Fabricated with Van Der Waals Bottom Contacts

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Effective control of 2D transistors polarity is a critical challenge in the process for integrating 2D materials into semiconductor devices. Herein, a doping-free approach for developing tungsten diselenide (WSe_2) logic devices by utilizing the van der Waals (vdWs) bottom electrical contact with platinum and indium as the high and low work function metal respectively is reported. The device structure is free from chemical disorder and crystal defects arising from metal deposition, which enables a near ideal Fermi-level de-pinning. With effective controllability of device polarity through metal work function change, a complementary metal-oxide-semiconductor field effect transistor inverter with a gain of 198 at a bias voltage of 4.5 V is achieved. This study demonstrates an ultrahigh performance 2D inverter realized by controlling the device polarity from using Fermi-level pinning-free vdWs bottom contacts.

1. Introduction

Transition-metal dichalcogenides (TMDCs) semiconductors have gained increased attention and investigated as a promising material for the next generation semiconductor electronic devices.[1,2] The ultrathin body realized by employing such semiconducting 2D materials offers a great potential for scaling the transistors by overcoming the short channel effect, providing an opportunity to further extend the Moore's law of the conventional silicon technology. Moreover, 2D van der Waals (vdWs) surface with free dangling-bonds free layers can be utilized effectively in combining several 2D materials for fabricating devices with diverse functions.[3–5] Recently, major progress has been made with 2D complementary metal-oxide-semiconductor (CMOS) consisting of one to be n-type metal-oxide-semiconductor (NMOS) (e.g., MoS_2, $MoSe_2$) and the other to be p-type metal-oxide-semiconductor (PMOS) (e.g., WSe_2 and BP);[3,6,7] nonetheless, homogeneous structures are preferable to heterostructures due to material uniformity and processing simplicity enabled by the same channel material. In the conventional Silicon (Si) technology, ion implantation has been used as an effective technique for controlling the device polarity (n-type or p-type) and doping concentration; however, the ion implantation cannot be employed effectively on 2D materials due to its atomic ultra-thinness to accommodate substitutional dopant atoms.

Recently, there have been tremendous efforts to build homogeneous 2D materials-based CMOS devices. Selectively doping the semiconductor channel which forms the homogeneous p-n junction for PMOS and NMOS,[8,9] for example, chemical charge transfer doping has shown promising progress. However, although homogeneous 2D CMOS devices have been developed through selective doping, its uncontrollability and temporal decay make it incompatible with the conventional CMOS fabrication platform presenting a great challenge in the device processing. Controlled polarity has been reported to enhance[10] 2D CMOSs functionality by depositing contact metals with various work functions through direct physical evaporation.[11] However, the fabricated devices still show indistinct controllability of polarity change regardless of the original work function of metals used; that is, Fermi-level pinning (FLP), which restricts the ability to control the device polarity (n-type or p-type) by contact engineering, presents a main obstacle to the effective application of 2D materials for realizing the CMOS functionality.[12] Several methods have been reported to modulate the polarity of 2D devices, including high work function interlayer,[13] ionic gating,[14] and dual-gate field-effect transistors (FETs).[15] Although most of the methods could not obey the Schottky–Mott rule because Schottky barrier height (SBH) formed at the metal-semiconductor interface doesn't vary as much as the change of metal work functions. Until now, a few novel methods have been tried to achieve Fermi-level depinning without introducing extrinsic dopants. One method involves making van der Waals contacts by transferring pre-deposited metal electrodes onto 2D materials using a dry transfer technique, which was demonstrated by Liu et al.[16] This method effectively prevents the physical vapor deposition-induced damage, which can introduce dopant levels in the bandgap of 2D materials as a pinning center. The other

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method involves making 1D edge electrical contacts to FETs as demonstrated in our previous research,[17] where 1D edge contact FETs use metallic edge states available at the 1D edge of a 2D material acting as a ultra-thin conducting metallic buffer between the metal and 2D material with a distance smaller than 1 nm. It is understood that the edges of the 2D materials have much lower density of states (DOS) compared with the contacting metals, giving rise to Fermi-level depinning, and therefore following Schottky-Mott rule. Recently, Kong et al.[18] reported that the transferred Au contacts have been integrated into a high-gain CMOS inverter, indicating the fabrication of high quality 2D materials-based CMOS logic transistors; however, direct metal deposition process is still used, which causes unwanted defects under electrical contact regions and changes the intrinsic properties of 2D materials. In addition, they reported that that the impact of the thickness of the WSe_2 on the polarity of the device is significant in the case where we use the surface contacts, whereas the impact of the thickness of the WSe_2 is not noticeable for the vdWs contacts. The sensitivity of the 2D semiconductors interface with the environmental factors or deposition process is carefully considered in previous research.[19–21] Therefore, it is critical to develop a device structure that has ultra-clean surface with metallic contact and shows tunability of the device polarity for realizing high-performance 2D CMOS devices.

In this work, we aimed at developing a CMOS device through a doping-free approach by utilizing the van der Waals bottom contact (vdWs BC) WSe_2 FETs with platinum (Pt) and indium (In) as the high and low work function metals, respectively. We fabricated a top gate FETs based on a hBN/WSe_2/hBN structure to enhance the performance of CMOS inverters and suppressing unwanted environmental influences. A consistent p-type channel with high hole mobility (50 $cm^2\ V^{-1}\ s^{-1}$ measured by four-probe method) and low sub-threshold swing (SS: 144 mV dec^{-1} measured by two-probe method) was developed by transferring a 2D material onto pre-patterned Pt contact (work function of ≈5.64 eV), while n-type channel was developed through the same method with pre-patterned In contact (work function of ≈4.1 eV) with 18 $cm^2\ V^{-1}\ s^{-1}$ electron mobility (measured by four-probe method) and 150 mV dec^{-1} SS (measured by 2-probe method). We understand that high electrical performances of our device are attributed to non-defect states vdWs BC and ultra-clean device surface sandwiched by hBN layers. The measured pinning factor (S) of our device at the metal–semiconductor (MS) contact was ≈0.93, which approaches the Schottky–Mott limit of 1.0, demonstrating the achievement of a Fermi-level pinning-free state.[16,17,22] This is again attributed to the controllability of the polarity change of WSe_2 by using vdWs BC. To the best of our knowledge, this is the first time effective utilization of the vdWs BC with metals of different work functions is effectively utilized for fabrication of functional CMOS devices. By controlling the device polarity using metals with different work functions, we achieved a logic inverter with a very high gain of 198 at V_{dd} = 4.5 V. Our research demonstrates a high-performance 2D CMOS inverter using vdWs BC without direct metallization or extrinsic doping such as charge exchange transfer and presents a novel method for tuning the device polarity only by metal work function engineering.

2. Results and Discussion

Figure 1 shows a schematic of our vdWs BC FET device with optical image of the device. For our device fabrication, bottom hBN flakes were mechanically exfoliated onto a heavily p-doped Si substrate with 300-nm of silicon oxide. The bottom hBN here is used to provide the ultra-flat and trap-free interface states with WSe_2. The bottom metal contact was pre-patterned on the bottom hBN flake by the electron-beam lithography and electron-beam evaporation. The exfoliated <10 nm thick WSe_2 and 20–50 nm thick top hBN were formed onto a sacrificial Si wafer. The pick and transfer technique[23] was utilized in the preparation of the vdWs BC devices. Finally, a local Ti/Au (5/100 nm) top gate is formed.

In contrast to our devices, the 2D devices with contact metal formed by direct physical evaporation are subject to the defects resulting from resist residues remaining from the subsequent lithography steps. Moreover, it is reported that the defects, unintentional doping and charge trap states are also induced during the direct metal deposition which causes FLP and degrades device performance.[12,24–26] Our vdWs BC approach overcomes the FLP, and controls the polarity of the WSe_2 FETs by contact engineering. First, the transfer of a 2D material onto the pre-patterned electrode avoids the high-energy involved direct deposition process which leads to the generation of defects and residues in the crystal structure of 2D materials. This can be confirmed by the cross-sectional high-resolution transmission electron microscopy (HRTEM) images shown in Figure 1c,d; ultra-flat MS interface without crystal defects or metallic clusters diffused into the 2D crystal structure can be seen.[27] Then, the ultra-clean top-gate FETs sandwiched by hBN eliminate defects, therefore, enabling an intrinsic performance of WSe_2.

We further examined the Fermi-level depinning effect of our device structure by evaluating the temperature dependency (in the range of 73 – 333K) of the electrical performance of FETs with metal contacts with different work functions: In (4.09 eV), titanium (Ti) (4.33 eV), gold (Au) (5.31 eV), palladium (Pd) (5.6 eV) and Pt (5.64 eV), ranging from 4.09 to 5.64 eV.[28] We performed two-probe measurements for all the WSe_2 devices prepared with the global top gate configuration. For our device structure with bottom contact electrodes, the polarity can be easily modulated from n-type to p-type by employing different work function metal electrodes. The transfer and output characteristics of the vdWs BC FETs with various metals from high to low work function are shown in **Figure 2**. From the transfer curves, we extract subthreshold swing, $SS = \frac{dV_{tg}}{d\log I_d}$. Also, four-probe measurement obtained for providing the accurate field-effect mobility (the detail of conductivity and mobility calculation are in Figures S1 and S2, Supporting Information, respectively). When WSe_2 contacts In with a work function of 4.09 eV, clear n-type behavior with low SS (150 mV dec^{-1}) and highest electron mobility (18 $cm^2\ V^{-1}\ s^{-1}$) is observed. According to the output curves (see Figure 2f), the In-contact device shows the Ohmic contact which is consistent with the negative SBH (see Figure S3a, Supporting Information), indicating that the In-contact device can be an excellent n-component for constructing a CMOS inverter. The devices with Ti electrode whose work function is ≈4.33 eV always show n-type dominant bipolar

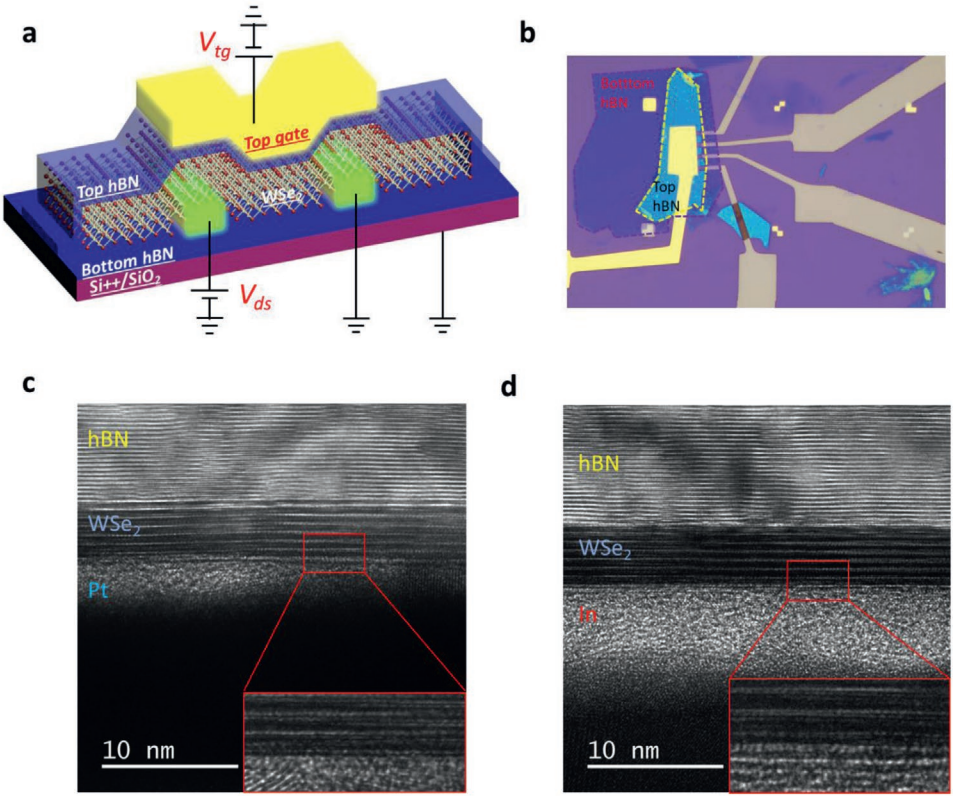

Figure 1. Fabrication process and cross-sectional HRTEM image of top gate vdWs BC FETs. a) The schematic and optical image of a top gate vdWs BC WSe_2 FET. b) Top gate vdWs BC WSe_2 device fabrication steps. c–d) Cross-sectional HRTEM image of the c) Pt- and d) In- contact devices with WSe_2 and hBN stacked, respectively. The enlarged views clearly show clean interface formed between WSe_2 and metals.

behavior, which is consistent with the WSe_2-Ti band alignment. Compared with In electrode device, Ti electrode device gives rise to output curves (see Figure 2g) which indicate the formation of Schottky contact. These results are consistent with that obtained from the temperature dependent transfer curves. SBH is also determined from the temperature dependent measurements shown in Figure S3b, Supporting Information, which is 64 meV below the conduction band edge. Compared with In electrode, the on-state current of the device with Ti electrode is about 100 times smaller, which also clearly indicates a larger SBH. Previously, p-type intrinsic WSe_2 FETs have been reported;[29,30] however, the reports mainly focus on electrical performances of the FETs but FLP has not yet been investigated for utilization in CMOS inverter fabrication. In this study, we also fabricated FETs using high work function metals. The demonstration of p-type intrinsic WSe_2 is more challenging and seldomly realized because of the FLP induced from interface states.[24–26] Herein, we test Au (5.31 eV) as the bottom electrodes, from which the fabricated device exhibits clear ambipolar behavior with an on-state hole current of approximately 1 μA μm^{-1}. Meanwhile, we found that the device presents Schottky contact, judging from the non-linear output curves (see Figure 2h). The SBH for Au electrode was is 120 meV for Au electrode (see Figure S3c, Supporting Information). When we changed the contact metal from Au to Pd (5.6 eV), we got a negative SBH of –15 meV from temperature dependent measurements of the Pd contact device. With the negative SBH (see Figure S3d, Supporting Information), the output curve of a Pd-contact device shows quasi-Ohmic behavior (see Figure 2i). When we employed Pt (5.64 eV) as a bottom electrode, we observed a p-type dominant electrical performance with high hole mobility (50 $cm^2 V^{-1} s^{-1}$) and the lowest SS (144 mV dec^{-1}) among all the tested metals. In addition, the output curve of the Pt-contact device is linear, indicating the formation of p-type Ohmic contact. The on-state current at 0.1 V source-drain bias reaches as high as 5 μA μm^{-1}. A SBH of –45 meV is also extracted using temperature dependent transfer curves (see Figure S3e, Supporting Information), indicating that the Pt work function is located below the WSe_2 valence band edge. This is very consistent with the experimental results, suggesting that Pt bottom electrode results in an effective p-type contact with negligible hole barrier. Additionally, these results reveal that Pt-contact device is suitable for integration into the CMOS inverter. Overall, the SS of our vdWs BC device is relatively low, close to the thermal limitation. Moreover, the mobilities of In, Au, Pd, and Pt are also high. We understand that the robustness of our devices is attributed to the defects-free vdWs BC and clean surface which allow us to implement our device structure for fabrication of high-performance CMOS inverter. Besides, we consider the impact of roughness of bottom electrode to the performance of the device which mentioned in previous research.[31] Figure S4a, Supporting Information represents the

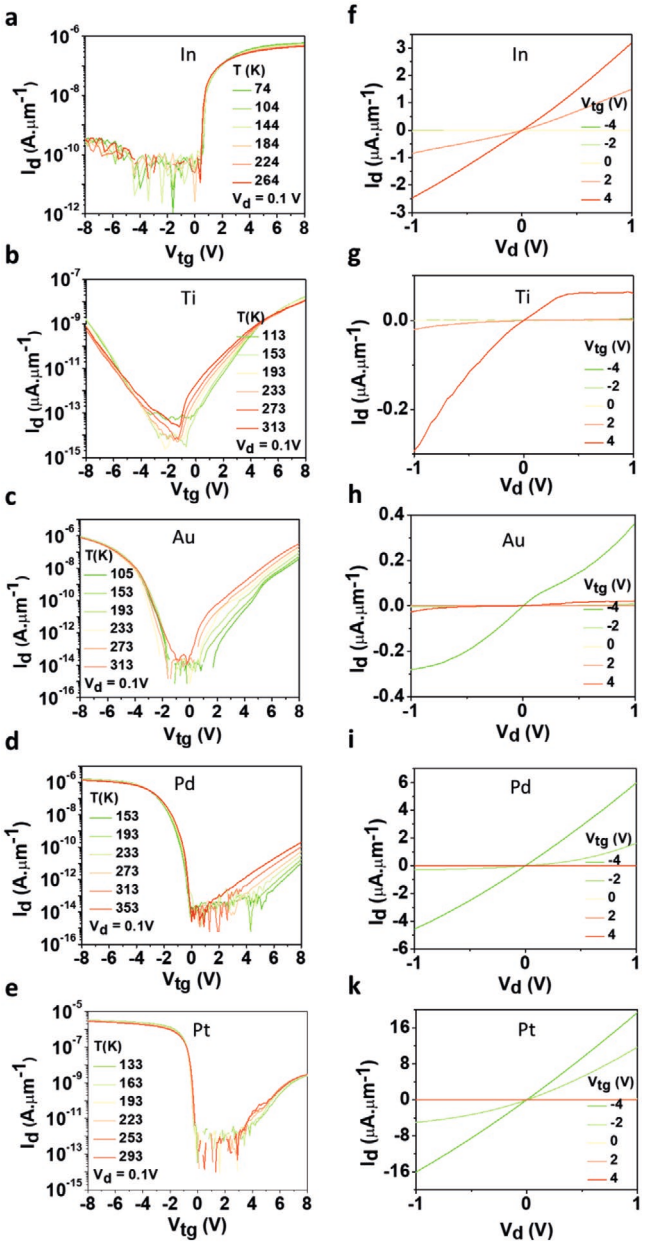

Figure 2. Electrical performance of the top gate vdWs BC FETs with different metal. a–e) Temperature dependent transfer curves of vdWs BC WSe_2 transistors at V_d = 0.1 V with a) In, b) Ti, c) Au, d) Pd, e) Pt. f–k) Output curves of vdWs BC WSe_2 transistors at V_d with f) In, g) Ti, h) Au, i) Pd, k) Pt.

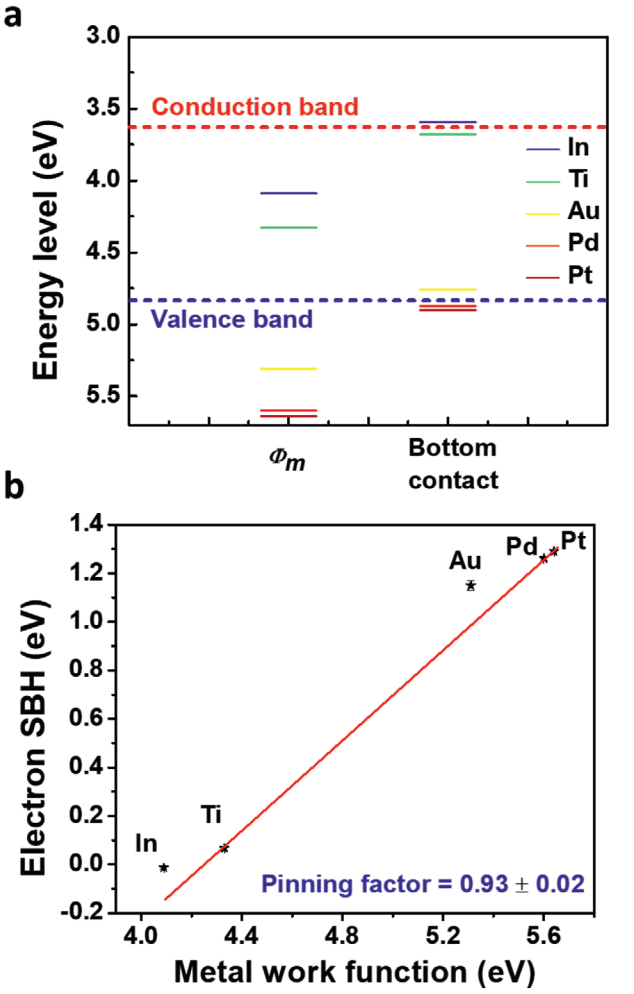

Figure 3. Metal–WSe_2 work function alignment and pinning factor of vdWs BC device. a) The metal–WSe_2 work function alignment according to the theoretical studies and our experimental results using top gate vdWs BC transistors. b) Experimentally determined SBH for various vdWs bottom metal contacts, where the SBH strongly depends on the metal work function (pinning factor = 0.93). Each data point has a very small error bar and represents the average SBH obtained from two or three tested devices, demonstrating its reliability.

roughness results of In and Pt electrodes, measured by atomic force microscopy (AFM). The roughness of In contact is found to be larger than that of Pt contact, and this could be partially responsible for the lower on-current of In contact with respect to Pt contact (Figure S4b, Supporting Information).

All the SBHs from In, Ti, Au, Pd, and Pt devices are shown in Figure S3, Supporting Information, being extracted based on thermal emission using the formula below:[32,33]

$$I_{ds} = AA^{*} \times T^{2} \exp\left[-\frac{\Phi_{SB}}{kT}\right] \quad (1)$$

Here, I_{ds} is the source-drain current. A is the junction area. A^{*} is the Richardson constant. K is the Boltzmann constant. T is the temperature. Note that all the SBHs extracted using this formula are determined from the flat band condition. In **Figure 3**a, the theoretical metal work function alignment within the WSe_2 band gap is shown. The Fermi-levels of In and Ti are located near the WSe_2 conduction band edge, whereas those of Au, Pd, and Pt are located near the WSe_2 valence band edge. Figure 3a shows the experimentally measured metal work function alignment within the WSe_2 band gap. The metal work function alignment in Figure 3a is found to follow the trend of theoretical prediction,[10] which indicates that the bottom electrode contact is effectively free of FLP. Compared with top electrodes, bottom electrodes prepared in this study are not subject to metal deposition by electron beam evaporation which induces dopant states at the metal–WSe_2 interface

arising from energetic metal atoms impinging onto the surface of WSe_2, giving rise to clear FLP-free metal–WSe_2 interface. Figure 3b shows the plot of the experimentally extracted metal work functions versus the theoretical metal work functions. The red line represents the linear fitting of the results, and its slope represents the pinning factor, S. When $S = 0$, Fermi-level is fully pinned at interface states position, whereas when $S = 1$, no Fermi-level pinning occurs. All the metal work functions are aligned, approximately following the Schottky–Mott rule. For the bottom electrode devices, the SBH mostly depends on the metal work functions. Moreover, the polarity of the devices can easily be modulated with metals of different work function from n-type to p-type, which has not been realized using top electrical contact devices. The pinning factor extracted from this study is around 0.93 ± 0.03 which is near the Schottky–Mott limit of 1.

To comprehensively examine the effect of Fermi level depinning effect of our structure, we extracted the tunneling transport mechanism by the plot of ln (I/V^2) against $1/V$ which consists of Fowler-Nordheim (F–N) tunneling and direct tunneling of the In and Pt contact device in Figure S5, Supporting Information. When the triangular-shaped barrier formed at the MS interface, the F–N tunneling occurs because hole or electron can sufficiently tunnel through the thin barrier; meanwhile, with trapezoidal-shaped barrier the direct tunneling happens instead. From the Equations S4 and S6, Supporting Information, we can realize that the plot of ln (I/V^2) against $1/V$ shows the logarithmic dependence while the direct tunneling occurs; Otherwise, with F–N tunneling it demonstrates the linear dependence with negative slope. From Figure S5a,b, Supporting Information we observed the opposite trends for low and high work function metal devices. With In-contact device, at positive gate bias the direct tunneling electron is the main conducting carrier because of negative SBH. Thus, the SBH for hole transport at negative gate bias is extremely high and formed a triangular-shaped barrier which allows the hole carrier to easily tunnel through the barrier. The same phenomenon happens with Pt-contact device. Since hole is the crucial conducting carrier, direct tunneling through a negative hole SBH takes place at negative gate biases and F–N tunneling as the main tunneling transport mechanism for electron takes place with high SBH at positive gate biases. The band alignment of tunneling mechanism of our device is shown in Figure S5c,d, Supporting Information. This observation is a strong evidence that Fermi level depinning happens with our device structure.

On the basis of Fermi-level depinning phenomenon from the application of vdWs BC which allows us for controlling device polarity, a complementary inverter can be built by utilizing the n-type and p-type FETs with a common top gate. We fabricated a dopants free WSe_2 inverter by employing In and Pt vdWs BC device as the N-MOSFET and P-MOSFET respectively. Both of the FETs are operated by top-gating with 25–30 nm thick hBN as the dielectric layer. The CMOS inverter structure is demonstrated in **Figure 4**a with a logic circuit diagram. The typical transfer characteristics of N-MOSFET and P-MOSFET are shown in Figure S6, Supporting Information which demonstrate consistent polarity controllability depending on metallic contacts used. Moreover, Figure 2f,k demonstrate the Ohmic behavior of both type of contacts, revealing the excellent contact performance of the device structure. Furthermore, the threshold voltage of both N-MOSFET and P-MOSFET is near 0 V, which indicates the presence of almost no trapped charges in the devices. The minimum subthreshold swing (SS) of N-MOSFET and P-MOSFET is 72 and 84 meV dec^{-1} respectively, which is close to the ideal thermal limitation of the FETs (60 meV dec^{-1}). The balance of threshold voltage and ideal SS between N-MOSFET and P-MOSFET is crucial to the construction of the high-performance inverter described below, from which we clearly observed the Fermi-level de-pinning phenomenon. Also, a p-n junction is obtained by adjoining two neighboring In and Pt electrodes. The rectification behavior is illustrated by current mapping in Figure S7, Supporting Information. Figure 4b shows the transfer characteristic of the inverter as a function of input voltage with V_{dd} ranging from 1 to 4.5 V, in which the sharp voltage transition is perceived with varying input voltage. The voltage gain, defined as gain = dV_{out}/dV_{in}, reaches a value of 198 at V_{dd} = 4.5 V (see Figure 4c). Dynamic inverter switching measure with V_{in} = 5 V under V_{dd} = 2 V at 50Hz is demonstrated in the Figure 4d which clearly shows logic function of inverter. Otherwise, we also demonstrate the dynamic inverter switching of our inverter at several frequency which shown in Video S1, Supporting Information. The threshold voltage and noise margin of our CMOS inverter are shown in Figure S8, Supporting Information. Our noise margin is over 80% for all of the measured supply voltage which shows large tolerance of our inverter to noise. Besides, when we have a closer look at the performance and the power consumption of our CMOS inverter (see Figure S9, Supporting Information), we find that dynamic power increases with increasing V_{dd}. For representing the reproducibility of our inverter, we also fabricated another CMOS inverter with metal and graphene as the top gate (see Figures S10–S12, Supporting Information) which also demonstrates similar performance. We compare the gain of our device with other 2D TMDCs inverter as the function of V_{dd}, in which our voltage gain shows the 2nd highest result. Moreover, the voltage gain of our device also higher than the commercial device performance.[34]

3. Conclusion

We developed a 2D WSe_2 logic devices through a doping-free technique which utilized a van der Waals bottom contact with Pt and In as the high and low work function metal respectively. The extracted pinning factor was ≈0.93 which is close to the Schottky–Mott limit, and therefore confirming the fabrication of FLP-free FETs. Moreover, by developing 2D P-MOSFET and N-MOSFET with the appropriate metal selection, we demonstrated a high performance CMOS logic inverter with the highest inverter gain of 198 (at V_{dd} = 4.5 V). Our research not only presents a high-performance CMOS inverter with a vdWs BC which avoids metal deposition, but also demonstrates a novel method for tuning the device polarity by metal work function engineering alone. Since WSe2 is understood to have similar electronic configuration and ban structure to other TMDC materials which are currently investigated, we expect the method presented in this work can be applied to other materials, although further research needs to be conducted for future utilization of vdWs BC for other 2D TMDCs.

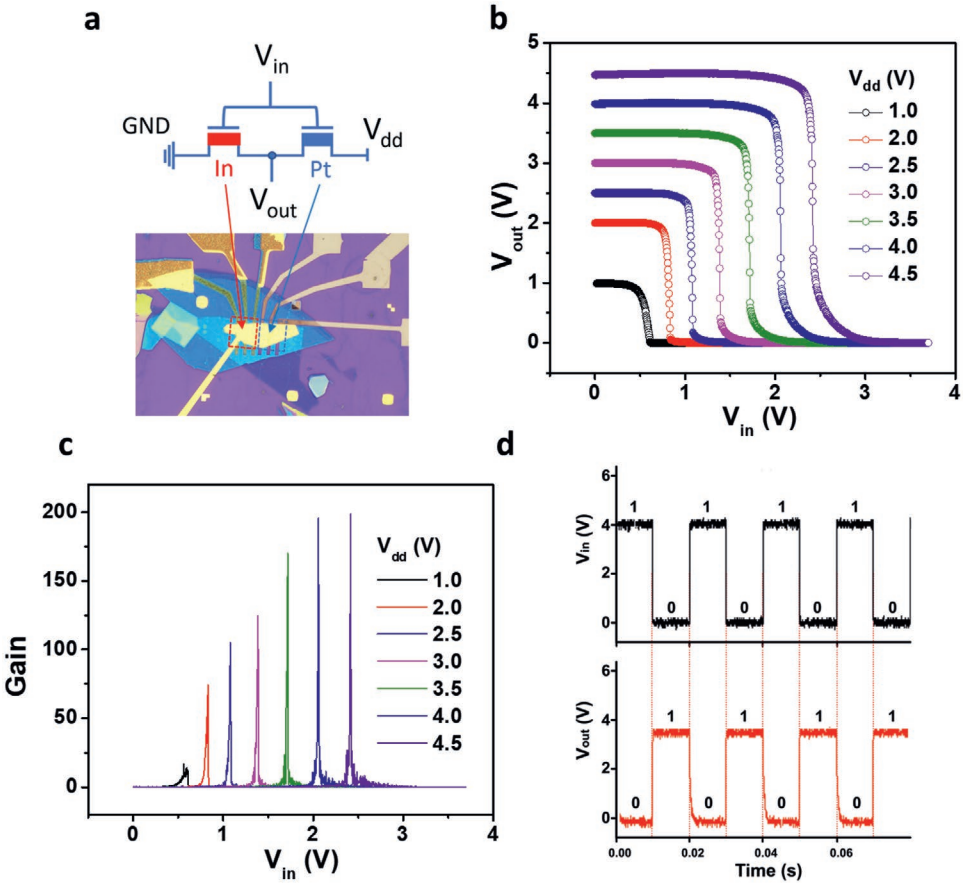

Figure 4. WSe_2 vdWs BC inverter. a) The optical image and circuit diagram of a WSe_2-based CMOS inverter with In (N-MOSFET) and Pt (P-MOSFET) vdWs BC. b) The voltage transfer characteristics of the inverter as a function of input voltage (V_{in}) for several supply voltages (V_{dd}). c) Voltage gain of the vdWs BC WSe_2-based inverter as a function of V_{in} for several V_{dd}. d) Dynamic output voltage response obtained from oscilloscope with input voltage from 4 V at 50 Hz under $V_{dd} = 4$ V.

4. Experimental Section

Fabrication of WSe_2 FETs: The WSe_2 thin flakes (thinner than 15 nm) were mechanically exfoliated from bulk WSe_2 (HQ Graphene) using Scotch tape. Prior to device fabrication, the heavily doped *p*-type Si wafers with SiO_2 as the dielectric layer (with a thickness of 285 nm) were cleaned thoroughly in acetone and isopropyl alcohol (IPA) in a sonicator for 20 min. The pristine few-layer WSe_2 was transferred onto a *p*-type Si/SiO_2 substrate. The WSe_2 flakes with the thickness < 10 nm were identified using an optical microscope. The metal contacts were patterned by electron-beam lithography (EBL) on a thin hBN substrate which was pre-exfoliated on Si/SiO_2 substrate and a metal electrode of Ti/Pt (Ti/In, Ti/Au, Ti/Pd, Ti) with the thickness of 5/15 (5/15, 5/15, 5/15, 20) nm was deposited using electron-beam deposition. Top gate 20–50 nm dielectric hBN and WSe_2 heterostructure were picked up and transferred using poly-carbonate film in glove box filled with inert gas. Finally, Ti/Au top gate electrode with the thickness of 5/100 nm is deposited.

Device Characterization: *Electrical Measurements*: All of the electrical measurements were performed using a semiconductor parameter analyzer connected to a 20 mTorr vacuum probe station.

Dynamic Inverter Switching Measurements: All the dynamic inverter switching was measured using a digital phosphor oscilloscope connected to a 20 mTorr vacuum probe station.

Atomic Force Microscope: The thickness of the top hBN was measured by using AFM (XE-100, Park system). AFM was performed by placing the sample on a metal puck, which was connected to the ground. The AFM image was taken at room temperature under atmospheric pressure and dehumidification condition (<25%) under noncontact mode.

Electron Microscopy to Measure the Interface of Metal-Semiconductor Contact: First, Pt and In – WSe_2 vdWs BC devices were fabricated on SiO_2/Si substrates using standard procedure as mentioned above. Then, focused ion beam milling was utilized for isolating a small portion of the contact, which was then moved to TEM grid for cross sectional HRTEM. The acceleration voltage for TEM measurement was 200 kV.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

bottom contact, complementary metal-oxide-semiconductors, Fermi-level depinning, top-gate field-effect transistors, tungsten diselenide (WSe_2)

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