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Traps at the hBN/WSe_2 interface and their impact on polarity transition in WSe_2

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Abstract

Semiconducting two-dimensional (2D) materials-based devices usually exhibit inferior electrical performance compared to their theoretical predictions, which is mainly attributed to the presence of high density of interfacial defect induced trap states within the bandgap of 2D materials. It is pertinent to control the density of interface traps (D_{it}) and identify their respective energy levels inside the band gap of the 2D materials to understand the tailored device performance. Here, we report the large modulation of D_{it} by electrical gating and varying the channel thickness of tungsten diselenide (WSe_2) placed on ultra-clean hexagonal boron nitride (hBN) gate insulator in a metal–insulator–semiconductor structure, which is revealed by performing multi-frequency capacitance and conductance measurements. Analysis of the 2D hBN/WSe_2 interface reveals that with the increase of WSe_2 thickness, D_{it} at the midgap of WSe_2 is reduced to 6×10^9 cm^{-2} eV^{-1}, which is less than D_{it} reported for SiO_2/Si interface ($\sim 10^{10}$ cm^{-2} eV^{-1}). Furthermore, by increasing thickness and applying gate voltage, D_{it} distribution is systematically modulated inside the WSe_2 band gap from valence band edge to mid-gap to conduction band edge, thereby changing the Fermi level of WSe_2, and inducing versatile device polarity. Our results show that D_{it} and its spatial energy distribution within the thickness tailored WSe_2 band gap primarily control polarity modulation in WSe_2.

1. Introduction

The semiconducting two-dimensional (2D) materials are considered a formidable choice for next-generation electronic applications, as thanks to their layered structure and dangling bond-free atomically smooth surface, 2D materials are expected to form high-performance miniaturized solid-state devices [1]. In reality, most of the ultrathin 2D materials-based devices exhibit compromised electrical performance, such as low carrier mobility, large sub-threshold swing, high off-state current (low on/off ratio), and strong Fermi level pinning [2, 3], which are significantly inferior to their theoretically reported predictions. Much more than that, 2D materials-based devices are notorious to exhibit large device-to-device variation under same operating conditions and suffer reproducibility issue [4]. These inferior and uncertain electrical characteristics are attributed to the presence of a large number of defects in 2D materials-based devices caused by several intrinsic (material imperfections, surface defects, dangling bonds) and extrinsic (substrate roughness, lattice mismatch, oxidation) sources [5]. These defects induce trap states that penetrate several nanometers deep inside the semiconductor [6]. The impact

of density of interface traps (D_{it}) is more severe in thin 2D materials as these atomically thin layers are completely depleted by trap states, which is unlike the bulk semiconductors. Therefore, D_{it} reflects the collective contribution of channel defects, and insulator–semiconductor and metal–semiconductor interface defects [7, 8]. Moreover, when compared to the metallic electrode at the metal–semiconductor interface in a conventional lateral device structure, the 2D channel shares a larger foot-print area with the gate dielectric at the insulator–semiconductor interface. Therefore, D_{it} at the insulator–semiconductor interface, predominantly dictate the device performance.

The 2D materials-based devices are reported to exhibit D_{it} ($\sim 10^{13}$–10^{12} cm^{-2} eV^{-1}) that is several orders higher than that of the ideal insulator–semiconductor interface ($<10^{10}$ cm^{-2} eV^{-1}) [5, 9]. Previously, some efforts have been made to control the D_{it} at the insulator–semiconductor interface in 2D material-based devices, by using different gate dielectric materials, such as bulk oxides (SiO_2, Al_2O_3, HfO_2) [10–12], atomically flat hexagonal boron nitride (hBN) [12, 13], and very recently, CaF_2 [14]. Among them, hBN as a gate dielectric is reported to induce relatively small D_{it} with 2D materials, thanks to its dangling bond-free ultra-clean surface [13]. Most of these studies are limited to a certain channel thickness, despite the fact that the thinner 2D flakes are more susceptible to the interface disorders than their thicker counterparts, because of their large surface-to-volume ratio [15], reduced density of states [16], and higher susceptibility of the gate dielectric-induced roughness [17]. In addition to controlling D_{it}, the particular energy of defect state inside the bandgap overwhelms the device performance by altering the band structure and doping profile in the 2D channel, and the band offset at the interface [6, 18–20]. For example, the chalcogen vacancy in semiconducting transition metal dichalcogenides, like MoS_2, WS_2, and WSe_2, induces trap states close to the conduction band edge, resulting in electron transport mainly [20–23]. Similarly, the traps at the dielectric/2D channel interface also induce different electrical response in 2D devices. For example, Na impurities at the SiO_2/MoS_2 interface create donor traps that are close to the conduction band, which results in *n*-type MoS_2. In contrast, the oxygen dangling bond-rich interface induces *p*-type response in MoS_2 by modulating the Fermi level near to the valence band [24]. Therefore, to exhibit tailored device performance, it is imperative not only to control the D_{it} concentration, but to modulate its respective energy in the bandgap.

Electrically, D_{it} can be characterized by performing current–voltage (I–V), capacitance–voltage (C–V) and parallel conductance–voltage (G–V) measurements on field effect transistor (FET) or metal–insulator–semiconductor (MIS) capacitor devices. The FET-based interfacial studies may lead to overestimation of D_{it}, because the channel charging process is dominated by the device resistance, rather than the carrier capture and release by the trap states [9], and includes the impact of the Schottky barrier [5]. On the other hand, C–V and G–V measurements at different frequencies can be more appropriate method to extract D_{it} over a wide energy range, by revealing the effects of channel defects and interface defects [7, 25, 26]. Therefore, we performed C–V and G–V measurements to a vertical MIS capacitors consisting of metallic Au electrode, insulating hBN, and semiconducting WSe_2. The vertical two-terminal MIS capacitor structure is effective at obtaining large capacitive area (of over 30 μm $\times$ 30 μm), and at suppressing the parasitic effect between probe pad and substrate, unlike the conventional lateral FET structure [12, 27, 28].

The C–V results obtained on different WSe_2 thickness-based MIS capacitors with hBN dielectric under varying gate voltage (V_G) and frequency (1 kHz–1 MHz) values show that as the thickness of WSe_2 increases from 4 to 27 nm, D_{it} at the WSe_2 midgap decreases from 1×10^{11} to 6×10^9 cm^{-2} eV^{-1}, and for thicker samples, remains constant. This unique trend is due to the competition between thickness of channel and screening length. Furthermore, the energy footprint of the D_{it} in WSe_2 band gap modulates from the valence band to the conduction band edge via mid-gap with applied gate bias and thickness increase, which accordingly results in Fermi level modulation in WSe_2, and thus contributes to the thickness-dependent versatile polarity (*p*-type, ambipolar, and *n*-type) in WSe_2 devices. In the section 2, firstly we discussed possible reasons of versatile polarity in WSe_2 and key factors responsible for frequency dispersion in depletion and accumulation regions. In next section, we extracted the D_{it} by C–V and G–V methods and plot the complete energy spectra of D_{it} for *p*-type, ambipolar and *n*-type WSe_2 to understand the modulation of polarity in WSe_2-based devices. The same methods can be used to understand traps induced in the devices fabricated using other 2D semiconducting materials like narrow band gap $MoTe_2$ or $MoSe_2$ and wide band gap WS_2.

2. Results and discussion

Figure 1(a) shows an optical image of the fabricated WSe_2-based vertical MIS and reference metal–insulator–metal (MIM) capacitors. More detail of the fabrication process is given in the experimental section, and in S1 of the supporting information (SI) (available online at stacks.iop.org/2DM/8/035027/mmedia). We carried out atomic force microscopy (AFM) analysis to determine the thickness and roughness of hBN and WSe_2 flakes, as shown in

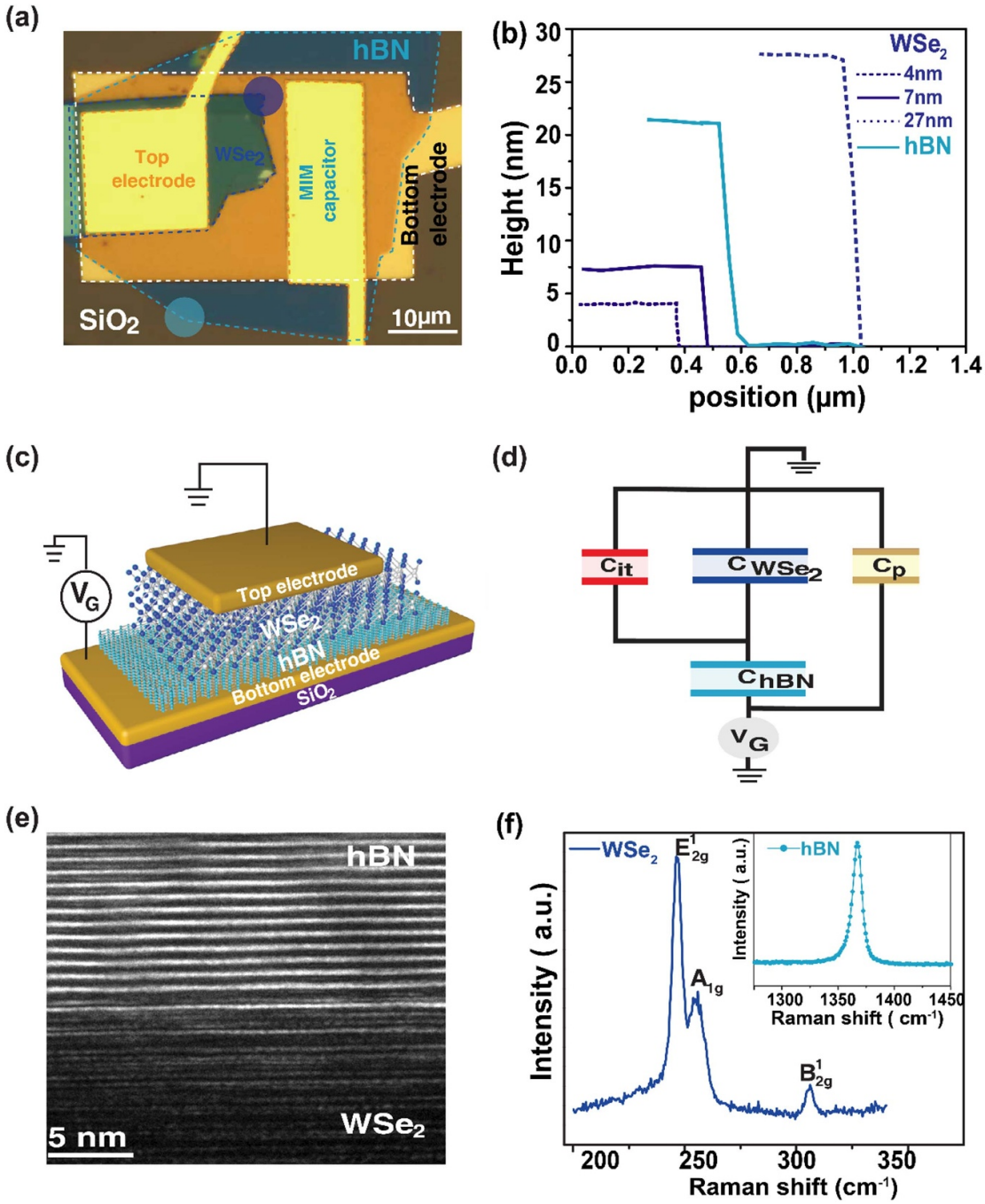

Figure 1. hBN/WSe_2 MIS Capacitor. ((a), (b)) An optical microscopic picture and flakes height profile measured by AFM along the dark blue and sky blue circle regions shown in (a), where dark blue lines represent the thicknesses of WSe_2 flakes, and sky blue represents the thickness of hBN flake. ((c) and (d)) represent the schematic of the fabricated vertical MIS capacitor devices and an equivalent circuit, respectively. (e) TEM image indicating the pristine interface between hBN and WSe_2 flakes. (f) Raman spectra of the multi-layer WSe_2 flake depicting characteristic peaks at 247, 256, and 306 cm^{-1}, corresponding to $E^1{}_{2g}$, A_{1g}, and $B^1{}_{2g}$, respectively. Inset shows the vibrational mode of hBN that appears at 1367 cm^{-1}.

figures 1(b), and S(2) of the SI. Figures 1(c) and (d) show a schematic and the equivalent circuit of the device, respectively. The obtained capacitance (C_t) is resulted from the cumulative effect of the hBN (C_{hBN}), WSe_2 (C_{WSe2}), parasitic capacitance (C_p) and the interface traps (C_{it}) which is associated with the applied frequency. The C_p further involves two sources: the stray capacitance originating from measurement setup and residual capacitance originating from the extra area of uncovered WSe_2 flake. For further details about C_p, see figure S(3) of the SI. The distortion-free interface is further confirmed by the transmission electron microscopy (TEM) image in figure 1(e), thanks to the facile polymer assisted pick-up technique; see figure S(1) of the SI. Prior to electrical characterization, the Raman spectra of the hBN/WSe_2 stack were collected at room temperature (RT), as shown in figure 1(f). The multilayer WSe_2 flake showed three representative vibration modes: in-plane mode ($E^1{}_{2g}$), out-of-plane mode (A_{1g}), and

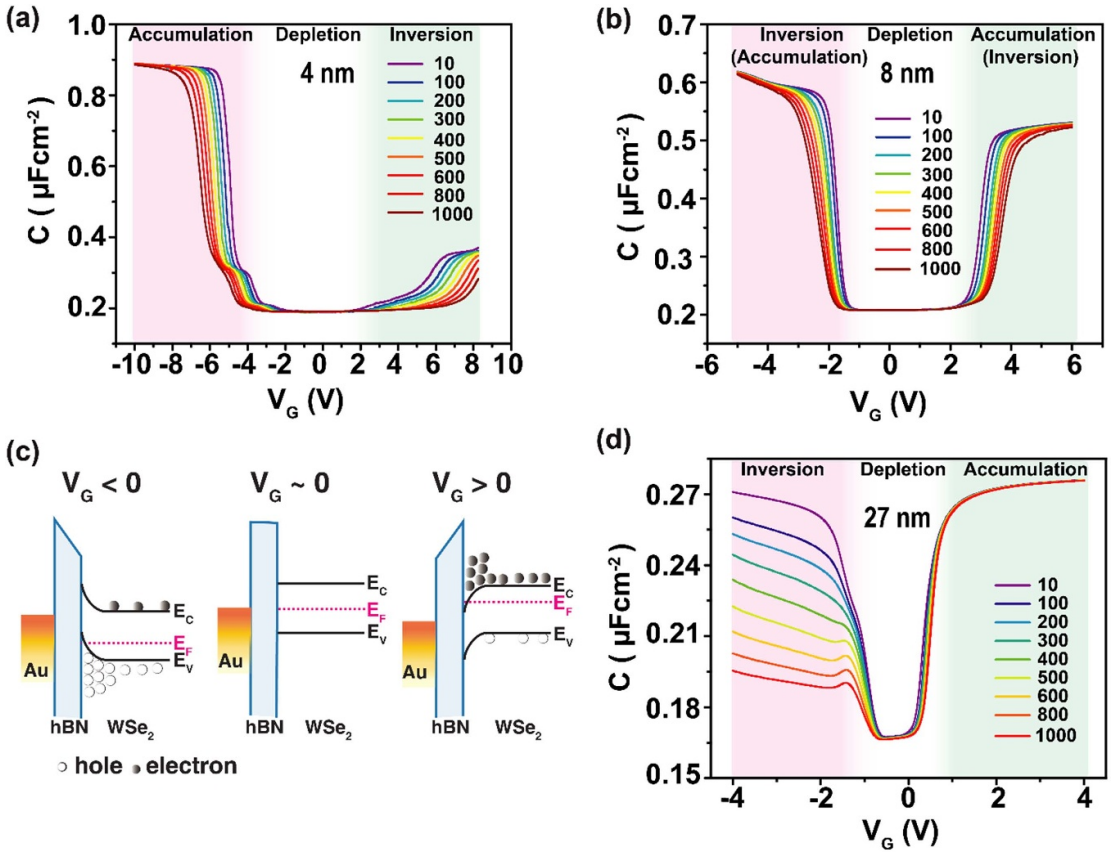

Figure 2. C–V characteristics for different thicknesses of the exfoliated WSe_2 MIS capacitor. C–V curves are obtained from ((a) 4 nm, (b) 8 nm, and (d) 27 nm) thick WSe_2 at various frequencies in kHz, depicting *p*-type, ambipolar, and *n*-type WSe_2 flake, respectively. Figure 2(c) shows the energy band diagrams of the ambipolar WSe_2 curves in respective regions at $V_G > 0$ V accumulation (inversion) region, ($V_G = \sim 0$ V) depletion region, and $V_G < 0$ V inversion (accumulation) region for electron (hole).

the mode due to interlayer interaction in multilayer flake ($B^1{}_{2g}$), which are spatially located at 247, 256, and 306 cm^{-1}, respectively. The inset in figure 1(f) is the Raman spectrum of hBN flake representing the E_{2g} vibration mode at 1367 cm^{-1} [29, 30].

2.1. Versatile polarity characteristics of WSe_2 devices

After physical characterization of the materials, we carried out the C–V measurements using an LCR meter on the devices with WSe_2 flakes of different thicknesses ranging from 4 to 61 nm. Extra efforts were put into using similar thickness (∼20 nm) hBN flakes. Before testing the MIS capacitors, we first measured the MIM capacitor consisting of Au/hBN/Au to determine the capacitance response of hBN alone; see figure S(4) of the SI. We have classified the measured MIS capacitors in three categories based on WSe_2 thickness; Group A: ⩽7 nm, Group B: 8–20 nm, and Group C: ⩾20 nm. First, the C–V results of a MIS capacitor with 4 nm thick (Group A) WSe_2 and 20 nm thick hBN were measured by sweeping V_G from −10–8 V and varying the frequency from 10 kHz to 1 MHz at RT, as shown in figure 2(a). At large negative V_G (<−5 V), the positive hole carriers accumulate at the WSe_2 surface, resulting in large capacitance ($C_{max} = \sim 0.9\ \mu F\ cm^{-2}$). With the increase of V_G (>−3 V), the channel is depleted of majority charged carriers, and thereby realizes smaller capacitance ($C_{min} = \sim 0.2\ \mu F\ cm^{-2}$). Afterwards, with the further increase in gating (>4 V), the device operates in weak inversion mode, with slight increase in capacitance due to the generation of minority carriers. This C–V trend attests a *p*-dominant (hole dominant) response of the thin 4 nm WSe_2, implying that the Fermi level is inclined toward the valence band edge of the WSe_2.

We then performed similar measurements using a multilayer WSe_2 flake i.e. 8 nm (Group B), as shown in figure 2(b). The obtained results show near-symmetric C–V trends at all measured frequencies from 10 kHz to 1 MHz, indicating the ambipolar response of the multilayer WSe_2. Alternatively, the Fermi level lies at the midgap in a multilayer WSe_2, and depending on the applied V_G, modulates toward conduction or valence band edge. When $V_G > 2.5$ V, the WSe_2 bands are bent downwards, resulting in the strong accumulation of electrons and the depletion of holes along the hBN/WSe_2 interface. However, when $V_G < -1$ V, the WSe_2 bands are bent upwards, resulting in the strong accumulation of holes and depletion of electrons along the

Table 1. Extraction of an electron (e) and hole (h) carrier density (N) and Debye Length (L_D) for various thickness of WSe_2 (t_{WSe2}) by graphical method at flat bad voltage (V_{FB}) using corresponding flat bad capacitance (C_{FB}).

		V_{FB} (V)		C_{FB} (F cm^{-2}) $\times 10^{-7}$		L_D (nm)		N (cm^{-3}) $\times 10^{16}$	
Group no.	t_{WSe2} (nm)	(e)	(h)	(e)	(h)	(e)	(h)	N_e	N_h
A	4	—	−4.86	—	4.73	—	8.01	—	8.22
	5	—	−5.53	—	4.21	—	8.41	—	8.14
B	8	2.95	−1.70	3.43	3.69	10.30	9.60	5.40	6.24
	14	6.90	−3.61	2.49	3.23	13.30	9.71	1.09	9.26
C	27	0.25	−1.42	2.01	2.32	17.70	15.30	1.84	2.47
	49	0.62	−0.91	1.58	1.51	22.40	23.50	1.15	1.06

hBN/WSe_2 interface. Therefore, the right (left) side of C–V plots in figure 2(b) represents the accumulation (inversion), while the left (right) side represents the inversion (accumulation) of electrons (holes). For the moderate V_G range i.e. −1–2.5 V, a nominal band bending occurs, representing a depletion region with $C_{min} = \sim 0.2\ \mu F\ cm^{-2}$. This is depicted in energy-band diagrams of the device given in figure 2(c).

To get more thickness variation, we tested a 27 nm thick WSe_2 (Group C) capacitor. To our surprise, the obtained results compiled in figure 2(d) depict n-type characteristics with strong accumulation of electrons for $V_G > 0.7$ V, and inversion of minority hole carriers for $V_G < -0.8$ V. These results indicate that the Fermi level in the 27 nm thick WSe_2 device is inclined toward the conduction band edge of WSe_2.

We fabricated WSe_2 devices of several different thicknesses in the range from 4 to 61 nm of the aforementioned thickness groups, to ensure the reproducibility of the diverse electrical results. From the obtained C−V results, we consistently realized three main findings. First, with the increase of WSe_2 thickness, the WSe_2 device polarity changes from p- to n-type. A fundamental mechanism responsible for the different polarity transition of 2D devices is still controversial and unclear [8]. Up to now it has reported that the polarity variation in 2D WSe_2 is mainly due to; (a) band gap modulation with the thickness: Previously, the thickness-dependent charge polarity modulation has been observed in lateral WSe_2 field effect devices using the same contact metal by tailoring the band gap of WSe_2 [31, 32]. Interestingly, our obtained results are close to the reported studies with a slightly different thickness range, which could perhaps be due to differences in the contact metal, device structure, measurement technique, and substrate. (b) Different work function metal electrodes: the various independent articles report diverse electrical characteristics of WSe_2 by contacting different work function metals [33–35]. In this work, we used the same metal (Ti) electrode and the thickness of WSe_2 was varying from 4 to 61 nm, therefore we can partially count the first reason and ignore the second. (c) Effect of insulator–semiconductor interface: It is reported that the different nature of interface traps at insulator–semiconductor interface in MoS_2 device can modulate the conductivity and Fermi level position [24]. This effect will be more prominent in thinner flakes, whose thickness is smaller than Debye screening length. Therefore, we think that the insulator–semiconductor interface predominantly contributes toward the versatile polarity in different thickness WSe_2 devices, and it will be the main focus of subsequent discussion.

Second, figures 2(a), (b) and (d) also show that the width of depletion region increases with the decrease of WSe_2 thickness. The high floor capacitance in the depletion region indicates that the thin WSe_2 flakes are fully depleted by charge carriers, such that the flake thickness remains smaller than the depletion width, which is around 20–40 nm for our WSe_2 devices; see figure S(5) of the SI. The full depletion of ultrathin 2D channels also poses limitations to extract carrier density from slope of $1/C^2$–V method [36]. Therefore, carrier densities for our thin WSe_2 devices are extracted using the graphical method, as listed in table 1: see figure S(6) of the SI for more details.

2.2. Frequency dispersion in hBN/WSe_2 based capacitor

Third, we observe increased frequency dispersion with decreasing WSe_2 thickness; also see figure S(7) of the SI. This is attributed to the several intrinsic and extrinsic device effects. (a) Band gap modulation with the thickness; it has been previously reported that the wider the band gap of a material, the stronger is frequency response [12]. Thinner WSe_2 flakes exhibit relatively wider effective band gap, which leads to the generation of very few thermally generated minority carriers with longer time constant at room temperature. Therefore, the negatively charged minority carriers cannot follow the very fast alternating field in a thin WSe_2 capacitor. As a result, the large frequency dispersion is realized. (b) The resistance effect; the access resistance contributed by the channel, the metal–semiconductor interface, and the parasitic components serves as a series resistance and collectively induces the frequency dispersion in accumulation region of device [2, 37]. The WSe_2 metal contact resistance is expected to increase by reducing thickness due to the increased band gap and corresponding barrier height [38].

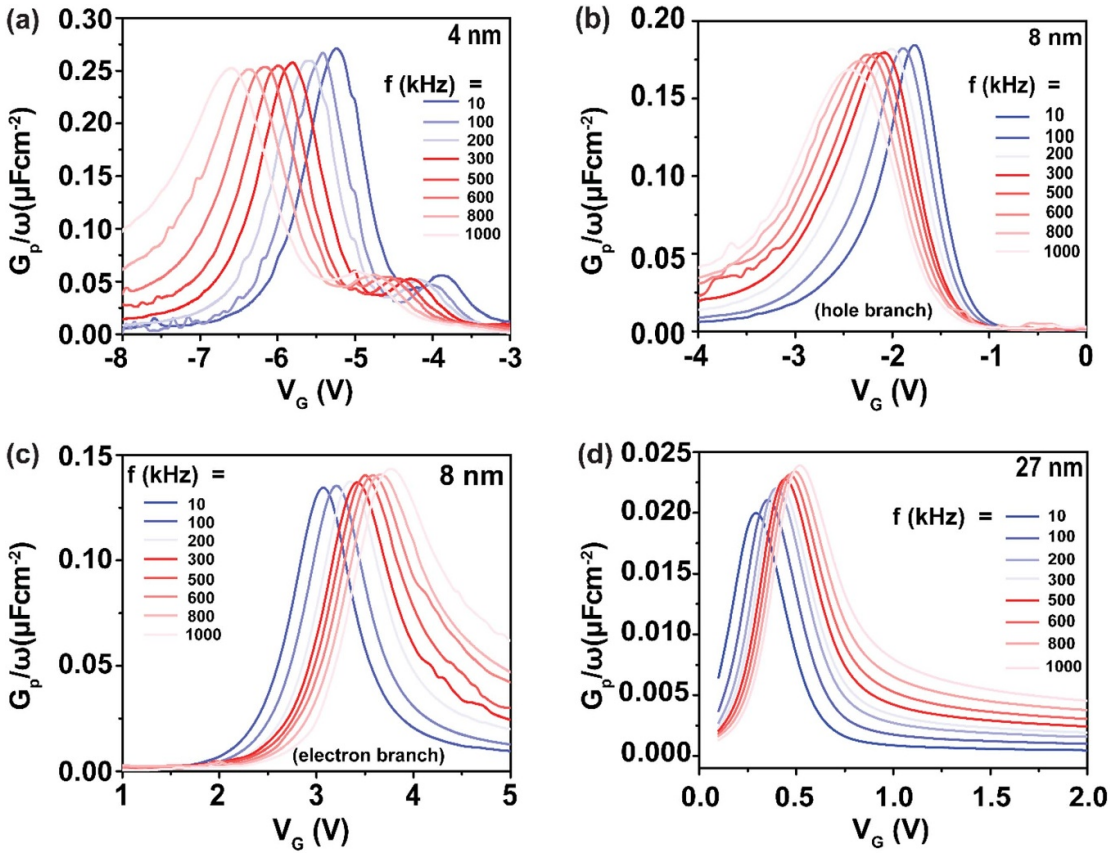

Figure 3. Normalized parallel conductance (G_p / ω − V_G) spectra of MIS capacitors of WSe_2 as a function of gate voltage at various thicknesses and polarities of (a) 4 nm thick *p*-type (b)–(c) of 8 nm thick ambipolar for hole (−4 ∼ 0 V) and electron (1 ∼ 5 V) dominant regions, respectively. (d) 27 nm of thick *n*-type.

Therefore, the large frequency dispersion observed in accumulation region in thin WSe_2 device is realized as compared to thick devices. Furthermore, the resistance effect will be more pronounced in FET device structures where charge carrier transport is controlled by channel and metal–semiconductor contact resistances, when compared to capacitor geometries [7, 37]. (c) The insulator–semiconductor interface; normally, the large frequency dispersion is attributed to the poor quality of semiconductor-gate dielectric interface [12, 25, 26]. Therefore, the increasing frequency dispersion trend in depletion region with decreasing WSe_2 thickness prompts us to evaluate third point in detail for all three WSe_2 thickness groups and understand its impact on electrical response.

2.3. Extraction of interface traps

The insulator–semiconductor interface can be qualitatively evaluated by probing the D_{it} from multi-frequency C−V and G−V curves, which are well known electrical methods developed for conventional devices, and these methods should be carefully employed for 2D devices [25, 26, 39]. The comparison between both methods can be found elsewhere [7, 37], and also see figure S(8) of the SI for detailed discussion. To obtain reproducible and confident results with additional information, we used both C–V and G–V methods to estimate the D_{it} along the hBN/WSe_2 in MIS capacitor geometry.

2.3.1. Extraction of D_{it} *by conductance method*

The conductive loss in depletion region is governed by the charging and discharging of defects, and therefore, G−V measurements provide the direct insight to the interface trap response of a device [7]. The angular frequency ($\omega = 2\pi f$) normalized parallel conductance (G_p) is plotted as a function of applied frequency in the respective depletion region V_G values for all three WSe_2 thickness groups in figures 3(a) and (d). More specifically, the G_p / ω − V_G plots shown in figures 3(a) and (b), are of 4 and 8 nm (hole branch) thick WSe_2 respectively while the graphs shown in figures 3(c) and (d), are of 8 nm (electron branch) and 27 nm thick WSe_2 respectively at given V_G and frequency values. The 4 nm thin WSe_2 device shows large G_p / ω peak (0.27 μF cm^{-2}) as compared to thick 27 nm WSe_2 device (0.023 μF cm^{-2}), suggesting the presence of large D_{it}, which is also consistent with the higher frequency dispersion observed in C–V curves for thin devices. Furthermore, the obtained G_p / ω − V_G plots exhibit the contrasting trend for electrons and holes dominant regions,

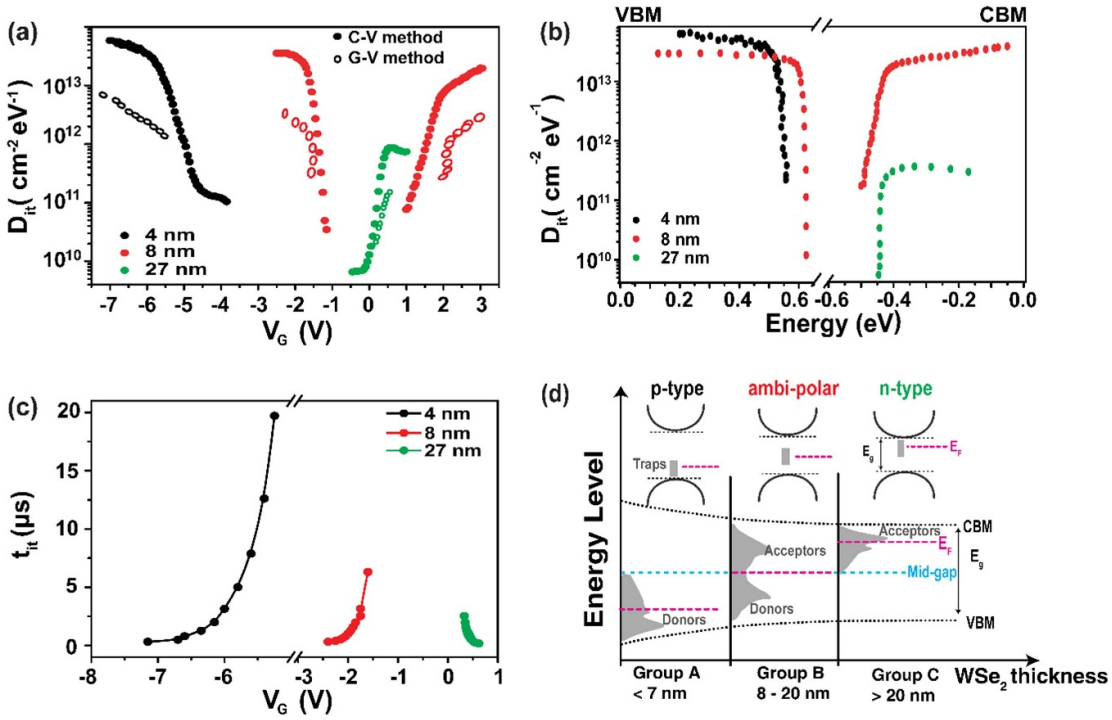

Figure 4. Complete profile of the interface trap density (D_{it}) of hBN/WSe_2 MIS capacitors. (a) Extracted D_{it} as a function of the applied V_G for 4 nm (*p*-type), 8 nm (ambipolar), and 27 nm (*n*-type) WSe_2. (b) The energy distribution of D_{it} for 4 nm (*p*-type), 8 nm (ambipolar), and 27 nm (*n*-type). (c) Extracted interface trap time constant as a function of applied V_G for 4 nm (*p*-type), 8 nm (ambipolar), and 27 nm (*n*-type) WSe_2. (d) Schematic to illustrate the distribution of D_{it} as a function of WSe_2 thickness in energy band diagram.

i.e. peak height decreases (increases) and the peak position shifts toward negative (positive) V_G for electrons (holes), implying the involvement of different D_{it} and different trap response time (τ_{it}) near conduction and valence band edges of WSe_2 respectively. This can be quantitatively evaluated by measuring D_{it} and their respective τ_{it} from G_p / ω peaks, which are correlated by the following equation [2, 12]:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right]. \quad (1)$$

Furthermore, D_{it} and their corresponding τ_{it} can be extracted from the G_p / ω peaks by using the following equations:

$$D_{it} = \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{peak}, \quad (2)$$

$$\tau_{it} = \frac{1.98}{\omega_o} \quad (3)$$

where $(G_p / \omega)_{peak}$ is the maximum value of normalized conductance peak, ω_o is the frequency at which $(G_p / \omega)_{peak}$ is obtained, q is the elementary charge, and A is the area of capacitor. From the conductance method, the obtained D_{it} for different WSe_2 thickness groups are shown in figure 4(a), where D_{it} range is limited to a certain V_G values only where the conductance peak is observed. Therefore, to realize the complete D_{it} spectrum in WSe_2 band gap, we used an alternative method (high and low frequency method) based on C−V results of figure 2.

2.3.2. Extraction of D_{it} *by capacitance method*

The capacitance-based (Castagne–Vapaille) method is applicable when D_{it} is assumed to be the primary source of frequency dispersion, which is the case for our device, as explained in section 2.2. The second assumption is that all D_{it} respond at low frequency and none of D_{it} respond at high frequency. It is difficult to correctly conclude, however, we can presume that maximum D_{it} is participating in C−V response at 1 kHz compared to 1 MHz, as presumed in previously published reports [25, 26, 39]. Thereby, device capacitance values at high and low frequency in the depletion region are used to extract the D_{it} using the following equation [25, 26, 39]:

$$D_{it} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{OX}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{OX}}\right)^{-1}\right] = \frac{C_{it}}{qA} \quad (4)$$

where C_{LF} and C_{HF} are the capacitance at low (1 kHz in this study) and high (1 MHz in this study) frequency, respectively, C_{ox} is the oxide capacitance and C_{it} is the interface trap capacitance. Figure 4(a) summarizes the obtained D_{it} values by both methods of all three thickness groups of WSe_2 as a function of

the applied V_G in the depletion region. The obtained D_{it} values using C−V and G−V methods follow the same trend, with small difference. This difference is obvious due to different assumptions which are considered to develop the Castagne–Vapaille model. Further detailed comparison among both the methods is provided in Gaur *et al* articles [7, 37]. The D_{it} values change exponentially with V_G for the three thickness groups, but with different trends. For the 4 nm thin WSe_2 device, D_{it} decreases from 5×10^{13} to 1×10^{11} $cm^{-2}\,eV^{-1}$ with the increase of V_G. For the 8 nm thick WSe_2 device, D_{it} first decreases from 3×10^{13} to 4×10^{10} cm^{-2} eV^{-1} for the hole branch, and then increases from 8×10^{10} to 2×10^{13} $cm^{-2}\,eV^{-1}$ for the electron branch with the increase of V_G. Finally, D_{it} increases from 6×10^{9} to 8×10^{11} cm^{-2} eV^{-1} with V_G for the 27 nm thick device. These results confirm that the thinner flakes are more susceptible to interface trap states.

2.4. Energy spectra of D_{it} for p-type, ambipolar and n-type WSe_2

The energy distribution of D_{it} can quantitatively picturize the band structure and the origin of D_{it} by assigning the energy values to the defect states using the given relation [7, 12]:

$$D_{it}(E) = D_{it,o}\, e^{\left(\frac{\Delta E}{\sigma}\right)} \tag{5}$$

where $D_{it,o}$ is the interface trap density at the midgap, ΔE is the energy difference between the minimum (maximum) of conduction (valence) band to the intrinsic Fermi energy of the semiconductor, and σ is the characteristic potential. We obtained $\sigma = 0.081$–0.094 eV for WSe_2 devices from the slope of D_{it} near the band edges; see figure S(9) of the SI. Figure 4(b) shows the measured D_{it} with respect to the energy band, wherein the minimum D_{it} values are at the midgap and increase toward the band edges. It is imperative to note that the D_{it} over wide energy window as given in figure 4(a) cannot be extracted by I−V measurements. For the 4 nm (27 nm) WSe_2 device, the D_{it} values increase toward the valence band (conduction band) edge. However, for the 8 nm WSe_2 device, the D_{it} first decreases, reaches the minimum value at the center, and then increases toward the band edges. It is interesting to note that the D_{it} modulation within the band gap of WSe_2 follows a similar trend to that of the Fermi level modulation for all three thickness groups.

Next, we compared the obtained τ_{it} using equation (3) as shown in figure 4(c), demonstrating that the τ_{it} variation over a large range of 0.3–20 μs as the thickness of WSe_2 is reduced from 27 to 4 nm. For 4 nm thin WSe_2 device, the τ_{it} varies from 0.30 to 20 μs and corresponding trap energy modulates from 0.20 to 0.50 eV from valence band edge. For the 8 nm thick WSe_2 device, the τ_{it} increases from 0.32 to 6.30 μs for the trap energy changing from 0.10 to 0.60 eV and 0.10–0.45 eV from valence and conduction band edge, respectively. Lastly, the τ_{it} increases from 0.34 to 3.2 μs with corresponding trap energy modulating from 0.25 to 0.45 eV from conduction band edge for 27 nm thick WSe_2 device. In brief, the obtained large modulation in D_{it}, their corresponding energy and τ_{it} of trap states strongly suggest that the different defects are active which contribute to the interface traps in different thickness WSe_2 devices. Figure 4(d) qualitatively summarizes this in a comprehensive energy band diagram. The band diagram elucidates that with the increase of WSe_2 thickness, the effective energy gap decreases, and the spatial energy location of interface traps and thereby Fermi level modulates from valence band side to the conduction band side, resulting in the polarity transition in WSe_2 from *p*-type to *n*-type with thickness. In group A (<7 nm) WSe_2 devices, the trap states having energy level close to the valence band edge are positive charge carrier traps, and act as donor like states. However, in group C (>20 nm) thick WSe_2 devices the negative charge carriers are transported from trap state to the conduction band edge and act as acceptor states, while group B (8–20 nm) devices exhibit both acceptors and donors like states.

2.5. Origin of D_{it} and its impact on electrical polarity

As mentioned earlier, the defect-induced trap states exhibit energy within the bandgap of the semiconductor WSe_2, and predominantly alter the device characteristics. Considering the channel defects, the freshly cleaved WSe_2 flakes are reported to exhibit a density of defect states of around 1.2×10^{12} cm^{-2} eV^{-1} due to the material imperfections, which are attributed to chalcogen vacancies, transition metal vacancies, antisites, and edge defects [20, 23]. The selenium defects induce the trap states that are 0.3 eV below the conduction band edge of WSe_2, and act as acceptor states, while the tungsten vacancies induce several impurity bands close to the valence band edge of WSe_2, and serve as donor states [20]. Therefore, the WSe_2 flakes with dominant transition metal (W) vacancies are reported to be *p*-type [20, 23]. Moreover, the selenium induced defects are reported to be populated abruptly due to short response time, while the tungsten induced defects are slow defects with large response time [40]. Therefore, our obtained results in figures 3(a) and (d) indicate the possibility of the presence of a greater proportion of slow tungsten traps (donor states) in the thinner WSe_2 flakes (*p*-doping) and the fast selenium traps (acceptor states) in the thicker flakes (*n*-doping), thus modulating the Fermi level and charge polarity in the WSe_2 accordingly. This statement seems unlikely, since all the devices are fabricated from the same parent flake, and no additional treatment is carried out on the WSe_2 flakes. However, WSe_2 is reported to exhibit both *n*- and *p*-type conductivity in the same

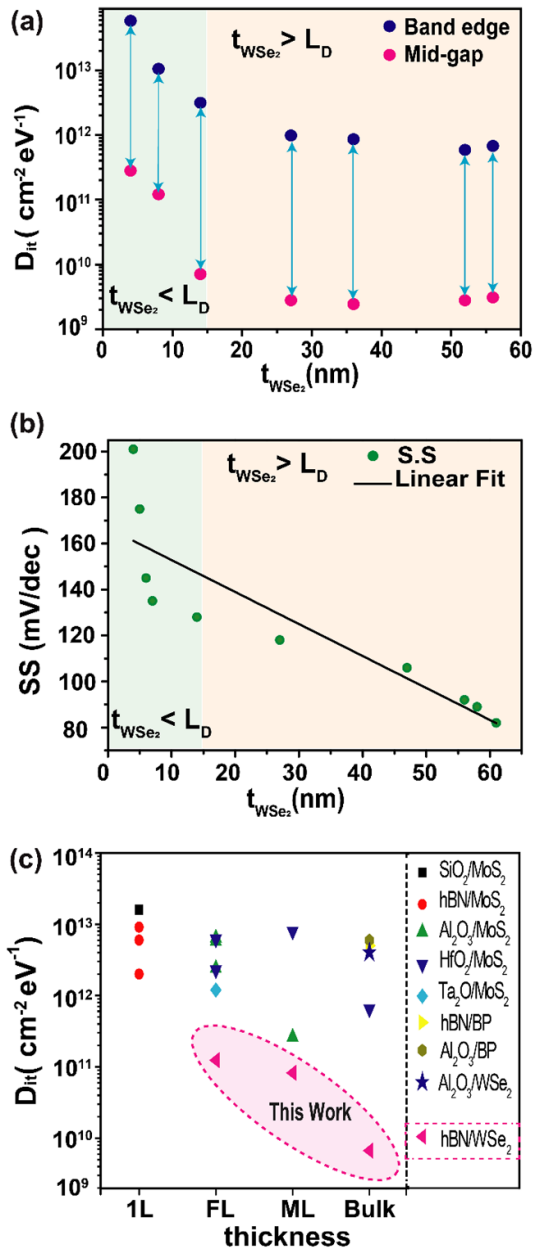

Figure 5. Thickness-dependence study. (a) Comparison of the obtained D_{it} from mid-gap (pink circles) to band edge (dark blue circles) for various thicknesses of WSe_2 from 4 to 56 nm, where sea green and cream color background areas represent the thickness of WSe_2 (t_{WSe2}) being less than and greater than the screening length (L_D), respectively. (b) Subthreshold swing (SS) as a function of WSe_2 thickness from 4 to 61 nm. (c) Comparison of minimum D_{it} values for different 2D materials dielectric interfaces [9, 12, 41–46], with those of the current work.

flake, due to the different nature of surface defect states [20].

Moreover, the interface traps at the dielectric/2D channel interface are also reported to modulate the conductivity and Fermi level in 2D materials [8, 24]. Our WSe_2 devices of different thickness are fabricated on ultra-clean hBN dielectric, and therefore we think that the dielectric induced surface roughness and strain effect is very small in our hBN supported WSe_2 devices. We plotted D_{it} for the diverse range of WSe_2 thickness (t_{WSe2}) in figure 5(a). Interestingly, the results show a monotonic decrease of D_{it} to 6×10^9 cm^{-2} eV^{-1} at the mid-gap (pink circle) with the WSe_2 thickness up to 27 nm and saturates afterwards. This unique trend can be understood by taking into account the Debye screening length (L_D) of the interfacial impurities in the WSe_2 channel, which is extracted by the following equation, [47, 48]:

$$L_D = \sqrt{\frac{\varepsilon_o \varepsilon_{WSe_2} k_B T}{q^2 N_{e,h}}} \quad (6)$$

where, k_B is the Boltzmann constant, T is the temperature, ε_{WSe_2} is the dielectric constant of WSe_2 [49], ε_o is the vacuum permittivity, and $N_{e,h}$ represents the electron and hole carrier density. For our WSe_2 devices, the estimated values of L_D are computed in table 1, when $\varepsilon_{WSe_2} = 4$–8 at $T = 300$ K and see figure S(6) of the SI for more details. When, t_{WSe2} is comparable to the $2L_D$, twice to account for the top metal–semiconductor and bottom insulator–semiconductor interfaces, the effect of interfacial impurities in the 2D channel will be dominant. On the other hand, when t_{WSe2} $2L_D$, the 2D channel will experience negligible influence from interface disorders. This is because the influence of intimate environment becomes weaker with increasing the thickness of flake due to the interlayer coupling effect [50]. The thinner WSe_2 flakes are prone to more interfacial defects caused by device processing-induced defects from the lithography and metal deposition over the 2D surface [51], and large substrate roughness induced-strain at the insulator–semiconductor interface as compared to the thicker flakes; therefore, we observe a decreasing D_{it} trend with channel thickness. This trend explains the compromised electrical performance, like degradation in mobility [17], and strong Fermi level pinning in thinner flakes, as compared to the thicker flakes [52, 53].

In addition to the carrier type modulation, D_{it}-induced interface trap capacitance ($C_{it} = q^2 D_{it}$) can affect the subthreshold swing (SS), which is the gate voltage required for one order change in the source-to-drain current. We compute the thickness-dependent SS of WSe_2 from D_{it} as [5, 9]:

$$SS = \ln 10 \frac{k_B T}{q} \left(1 + \frac{C_{dep} + qD_{it}}{C_{ox}}\right) \quad (7)$$

where C_{dep} are the capacitance in depletion region. Figure 5(b) shows the results obtained, where with the increase of WSe_2 thickness of the device from 4 to 61 nm, the maximum SS decreases monotonically from 201 to 82 mV dec^{-1}. It is imperative to note here that, the SS values sharply increase when the thickness of WSe_2 approaches to the screening length ($t_{WSe2} < L_D$) which indicates that the thinner flakes are more susceptible to the external perturbations induced from insulator–semiconductor and metal–semiconductor interfaces. Therefore, the large

SS value is realized in thinner WSe_2 devices. These results also suggest that there remains ample room to further optimize the interface quality by reducing D_{it} to achieve low SS, close to the ideal value of 60 mV dec^{-1}. The D_{it} in 2D materials-based devices can be greatly reduced by growing high-quality materials to realize low intrinsic material and surface defects, using an ultra-smooth dielectric like hBN and CrF_2 to suppress dielectric-induced roughness, by transferring prefabricated metallic electrodes, using graphite contacts and hBN encapsulated device geometry to control the device processing induced defects [5, 15, 34]. Moreover, the effect of D_{it} on device polarity can be harnessed to fabricate complementary devices with different thickness WSe_2 channel for high-performance electrical and optical devices. Lastly, figure 5(c) compares our obtained D_{it} values to those in the literature. Interestingly, when compared to the reported values for other 2D materials, our WSe_2 devices show smaller D_{it} at the mid-gap [9, 12, 41–46]. In particular, the thick WSe_2 (>27 nm) device on hBN dielectric showed lowest D_{it} of 6×10^9 cm^{-2} eV^{-1} at the mid-gap, which is several order smaller than that of conventional (SiO_2, HfO_2, and Al_2O_3) and 2D materials interfaces and comparable to Si/SiO_2 interface. More importantly, the smaller D_{it} values in our devices are attributed to the better quality exfoliated 2D materials, ultraclean and atomically smooth hBN/WSe_2 interface, and facile polymer-assisted transfer on predeposited metal electrode.

3. Conclusion

We studied the interfacial properties of different thickness WSe_2 flake with hBN gate dielectric and their effect on device performance. The thickness-dependent interface characteristics show that the concentration and the corresponding energy footprint of D_{it} are modulated inside the WSe_2 band gap with electrical gating and channel thickness variation, and therefore contribute to the electrical modulation in WSe_2. We provide the complete picture of D_{it} distribution in the band gap of WSe_2, and its impact on polarity modulation in WSe_2-based devices. This study will be helpful to optimize the channel thickness through understanding the importance of defect states controllably modulating the electrical response to fabricate controllable and high-quality devices.

4. Methods

4.1. Devices fabrication

We fabricated a vertical MIS heterostructure capacitor, as shown in figures 1(a) and (b). Firstly, we defined the bottom electrode area of 80 μm × 50 μm by using electron beam lithography on p-type silicon substrate covered with thermally grown 285 nm SiO_2, and deposited 5/25 nm thick Cr/Au electrodes by using electron beam deposition (EBD) under high vacuum (8×10^{-8} Torr), to ensure good electrical contacts. Subsequently, we exfoliated hBN and WSe_2 flakes mechanically on Si/SiO_2 substrate separately. Optical microscopy was used to select a clean and uniform thickness of hBN and WSe_2 flakes. The transfer stage inside the glovebox was used to position and transfer the selected hBN and WSe_2 flakes to precisely stack on a target bottom electrode. Finally, 5/80 nm thick Ti/Au metal electrodes were deposited as a top electrode, using the standard EBD technique.

4.2. Device characterization

4.2.1. Atomic force microscopy (AFM)

All the AFM analyzes were performed at RT under atmospheric pressure by placing the sample on a metal puck that was grounded.

4.2.2. Transmission electron microscopy (TEM)

The cross-sections of MIS heterostructure were prepared in a focused ion beam system. A sharp layer of Pt on the surface of the chosen location was deposited for passivation during milling, as well as providing mechanical stability to the cross-sectional slice after its removal. Subsequently, TEM analyzes were performed using Cs-corrected high-resolution TEM.

4.2.3. Electrical (C–V) and (G–V) measurements

After completing fabrication, the electrical measurements were conducted using a parallel mode of the LCR meter in a vacuum chamber at RT.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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