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Metal–Insulator Transition Driven by Traps in 2D WSe_2 Field-Effect Transistor

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Localized trap density (D_t) at the 2D channel–gate dielectric interface and its relative strength to carrier–carrier interactions depending on the thickness of the 2D channel can determine the nature of a metal–insulator transition (MIT) in 2D materials. Here, the MIT occurring in WSe_2 devices is systematically analyzed by varying the WSe_2 thickness from ≈20 nm to monolayer to explore the effects of D_t on MIT. The corresponding critical carrier density increases from $\approx 8.30 \times 10^{11}$ to 9.45×10^{12} cm^{-2} and D_t from $\approx 6.02 \times 10^{11}$ to 1.13×10^{13} cm^{-2} eV^{-1} as WSe_2 thickness decreases from ≈20 nm to monolayer. These large increments in D_t with decreasing thickness of WSe_2 induce a strong potential fluctuation in the band of WSe_2, causing charge density inhomogeneity in the system, which attributed to tuning the MIT. The critical percolation exponent is strongly dependent on WSe_2 thickness with an excellent agreement between the transport data and percolation theory achieved from thinner WSe_2 devices, while the transport data measured from multilayer WSe_2 devices does not obey the percolation theory. These results suggest that the nature of MIT strongly depends on the WSe_2 channel thickness and corresponding unscreened charge impurity and strength of D_t at the interface.

1. Introduction

Technically, atomically thin 2D materials are all surfaces and interfaces.[1–5] Therefore, 2D materials-based devices exhibit a trap density (D_t) of ≈10^{13} – 10^{12} cm^{-2} eV^{-1} that is several orders higher than that of high-quality channel-gate dielectric interfaces at <10^{10} cm^{-2} eV^{-1}.[6,7] Thus, the intrinsic characteristics of 2D material-based devices are readily tailored by their interfacial quality.[8,9] More specifically, carrier transport within a channel is significantly influenced by the localized state commonly known as the trap states at the 2D channel–gate dielectric interface by inducing transport through interface trap charges.[7,10] These electrically active interface traps can adversely affect device performance by reducing charge carrier mobility, increasing subthreshold swing, and enhancing off-state current (reducing on/off ratio).[7] In addition, these charge impurities near the surface of 2D materials and different kinds of disorders can strongly suppress electronic interactions and control the electrical characteristics of the system.[11–13] Since the pioneering observation of metal–insulator transition (MIT) phenomena in 2D systems, carrier–carrier interaction has been widely considered as the driving force of MIT from the viewpoint of quantum phase transition.[14–16] However, the previous theories suggested that the relative strength of D_t and carrier–carrier interaction in the system determine the physical origin of MIT.[17–20] In 2D layer materials, the strength of carrier–carrier interaction and disorders induced by interface traps, and defects can be modulated by controlling the thickness of the 2D channel, substrate engineering, and surface passivation.[2,21] In general, carrier–carrier interactions decrease with reducing thickness while localized D_t increases significantly. Therefore, different kinds of transition mechanisms in 2D layered materials are expected depending on the thickness of the flake and the corresponding interface quality. Previously, it has been reported that the D_t drastically increases when employing thin flakes since thinner 2D flakes are more susceptible to interface disorders than their thicker counterparts.[6,7,22] Thus, it is difficult to correctly identify the origin of MIT in a 2D material system when both carrier-carrier interactions and a large amount of localized trap states (≈10^{13} cm^{-2} eV^{-1}) induced from the channel and channel–gate dielectric interface effects come into play.

In the past, some efforts have been made to explain the MIT in 2D MoS_2,[23–26] ReS_2,[27] CuInSe,[28] and WSe_2.[29] However, most of these studies were limited to a certain channel thickness. Although a few studies have reported MIT in 2D materials,[23,26–30] how localized D_t interplays near a transition point with varying thickness of 2D flakes remains unclear. There is a need to systematically analyze the underlying mechanism of MIT with different thicknesses of 2D channels. Therefore, the objective of this study was to systematically investigate the MIT behavior observed in 2D WSe_2 devices by varying the thickness

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of the WSe_2 flake from ≈20 to 0.73 nm (monolayer), different from previous studies.[23,27,29] We carried out multifrequency capacitance–voltage (MFC-V) and transport measurements with temperatures ranging from 300 to 75 K to determine the effect of interface quality and correspondingly localized D_t on MIT. Since MFC-V measurements carried out by applying different excitation frequencies (1 kHz to 1 MHz in this study) provide direct insight about localized D_t, they are considered the most appropriate and powerful technique to analyze the channel-gate dielectric interface and its impact on device characteristics.[22,31–33]

This thickness-dependent systematic analysis provided an interesting clue that the MIT point strongly depended on flake thickness. The corresponding critical carrier density (n_c) at the transition point significantly increased with reducing WSe_2 channel thickness. These tunable characteristics of WSe_2 devices can be used for fast optoelectronic switches by utilizing the difference in optical transmission between insulating and metallic regions. To further understand this thickness-dependent tunable transition in WSe_2 devices, we analyzed the interface between the channel (WSe_2) and gate dielectric (hBN) by estimating localized D_t in all measured devices. We found that the occurrence of MIT in WSe_2 devices strongly depended on the interface quality and corresponding localized D_t at the interface. Moreover, we analyzed our data of WSe_2 devices with different thickness of WSe_2 flake by employing the percolation model of conductivity. Based on thickness-dependent percolation analysis that follows the principle of power-law (i.e., $\sigma\ (n) = A(n - n_{cp})^{\delta}$), we obtained values of percolation exponent δ ≈1.377 ± 0.013 to 1.4257 ± 0.022 for monolayer (0.73 nm) and δ ≈1.743 ± 0.057 to 1.966 ± 0.052 for few layers (3.16nm) in WSe_2 devices at measured temperatures of 75 to 300 K. These obtained values of δ in WSe_2 devices using up to a few layers of WSe_2 are close to the expected δ value in 2D materials, suggesting that MIT occurring in thinner (up to a few layers) WSe_2 devices is a percolation driven transition. In contrast, transport data of multilayer WSe_2 devices did not obey the percolation theory, implying that interaction-dominant MIT occurred in multilayer WSe_2 devices. In addition, the Wigner–Seitz radius (r_s) significantly decreased from ≈8.60 to 2.20 with decreasing flake thickness from multilayers to monolayer. This also indicates that Coulomb interaction between carriers becomes weaker with decreasing thickness and the system highly becomes disordered.

2. Results and Discussions

Figure 1a,b illustrates schematic and optical images of a specially designed van der Waals bottom contact field-effect transistor (FET) fabricated by transferring mechanically exfoliated flakes of WSe_2 and hBN on the pre-deposited source and drain electrodes (Pt) on a p-type silicon substrate coated with 285 nm SiO_2. Further details of the van der Waals bottom contact FET fabrication process are given in the device fabrication section, and S1 of Supporting Information. Here, we used pre-deposited bottom electrodes to avoid chemical disorder and crystal defects induced by direct lithography and metal deposition on the WSe_2 channel. The equivalent circuit of devices shown in Figure 1c demonstrates total measured capacitance (C) resulting from the

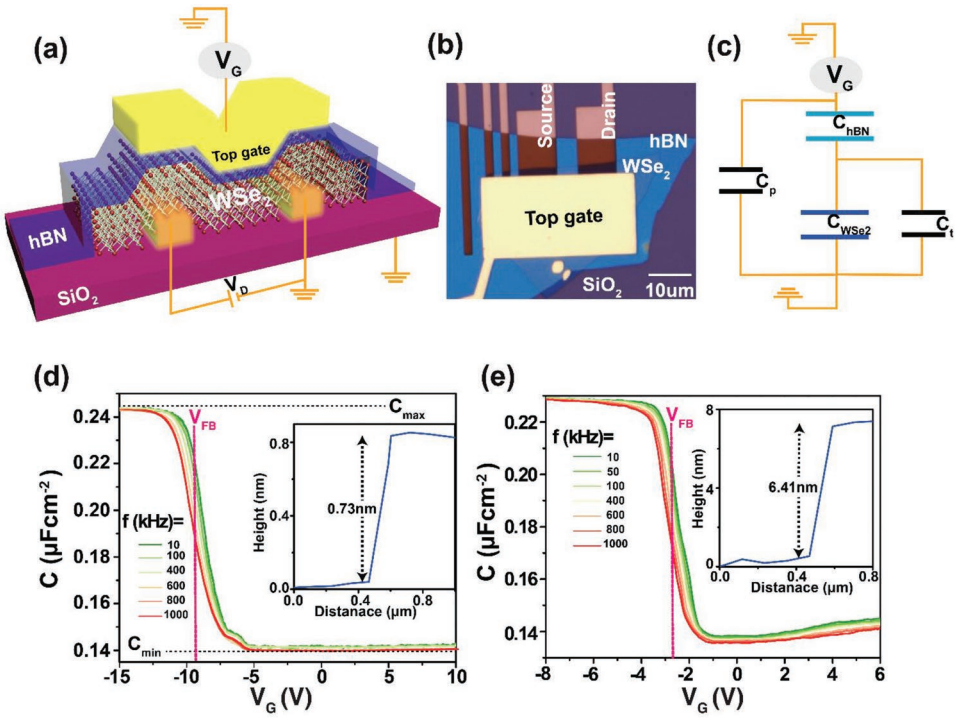

Figure 1. Device fabrication details and frequency-dependent capacitance-voltage measurements. a–c) Schematic image and optical image, and an equivalent circuit of the top gate van-der-Waal bottom contact WSe_2 field-effect transistor, respectively. d,e) show the capacitance-voltage characteristics obtained from a monolayer (0.73 nm) and multilayer (6.41 nm) WSe_2 devices at various frequencies, respectively, where the dotted pink verticle line indicates the flat band voltage (V_{FB}). Thickness height profiles of WSe_2 flakes taken by AFM of respective devices are shown in the inset of (d) and (e).

collective effect of the hBN (C_{hBN}) and WSe_2 (C_{WSe2}) in serial connection plus parasitic capacitance (C_p) and trap induced capacitance (C_t) in parallel connection. For further details about C_p and the equivalent circuit, see Figures S2 and S3 (Supporting Information), respectively. Before electrical characterization, we carried out atomic force microscopy (AFM) analysis to ascertain the thickness of flakes and surface roughness. AFM height profiles are shown in the inset of Figure 1d,e. Details are given in Figures S4 and S5 (Supporting Information).

2.1. Capacitance-Voltage Measurements

Multifrequency capacitance-voltage (MFC-V) measurements[32] were carried out inside a vacuum chamber using an LCR meter by applying the gate voltage (V_G) and varying the applied frequency from 10 kHz to 1 MHz at room temperature (RT) on WSe_2 devices with the thickness of WSe_2 flake varying from ≈20 to 0.73 nm (monolayer). Extra efforts were put to use similar thickness≈20 nm of the hBN flakes. Figure 1d,e shows MFC-V results of monolayer and 6.41 nm thick WSe_2 devices, respectively. When V_G is smaller than V_{FB} (where V_{FB} is flat band voltage), holes accumulated at the WSe_2/hBN interface and the obtained capacitance approached hBN capacitance $C_{max} = C_{hBN}$. Whereas when V_G is larger than V_{FB}, holes started to deplete from the WSe_2/hBN interface and the measured capacitance becomes $C_{min} = \frac{C_{hBN} C_{WSe_2}}{C_{hBN} + C_{WSe_2}}$ in the deep depletion region. The obtained V_{FB} of ≈− 9.3V for 0.73 nm and − 2.79V for 6.41 nm thick WSe_2 devices estimated by employing the graphical-based method.[34,35] For details see Figure S6 (Supporting Information). Frequency dispersion in the depletion region is attributed to the presence of traps at the WSe_2/hBN interface.[22,32,33] Furthermore, the traps at the WSe_2/hBN interface will be discussed later by quantifying the localized traps density (D_t).

We then performed temperature-dependent measurements in the range of 75 to 300 K with a step of 25 K to examine the response of capacitance-voltage (C-V) of the above-mentioned thickness range (20 nm to monolayer) of WSe_2 devices. C-V curves of WSe_2 devices with different thicknesses obtained at various temperatures showed an interesting metal-insulator transition (MIT) phenomenon at a certain V_G.[23,24] For example, 7.23 nm and 3.16 nm thick WSe_2 devices show MIT points at V_G of = − 3.6V and − 6.4V as shown in **Figures 2**a,b, respectively. Below the MIT point, the capacitance increased with increasing temperature, indicating the formation of an insulating phase. However, above the MIT point, temperature dependency is the opposite, showing characteristic of the metal. To visualize the change in capacitance with V_G and temperature, we mapped capacitance data of 7.23 nm thick WSe_2 devices as shown in Figure 2c. The color plot data confirmed distinct regions: $\Delta C/\Delta T > 0$ when V_G ≈>− 3.6 V indicating insulating phase, $\Delta C/\Delta T$≈0 at V_G ≈− 3.6 V suggesting temperature-independent point, and $\Delta C/\Delta T$ <0 when V_G ≈<− 3.6 V showing the metallic phase. The corresponding critical carrier density (n_c) at MIT point is n_c ≈2.08 × 10^{12} cm^{-2} (V_G = − 3.6 V) for 7.23 nm thick WSe_2 and n_c ≈6.81 × 10^{12} cm^{-2} (V_G = − 6.4 V) for 3.16 nm thick flake. It is estimated with $n_{2D} = \frac{C_{ox}(V_G - V_{th})}{q}$, where C_{ox} is the oxide capacitance per unit area, V_{th} is the threshold voltage,

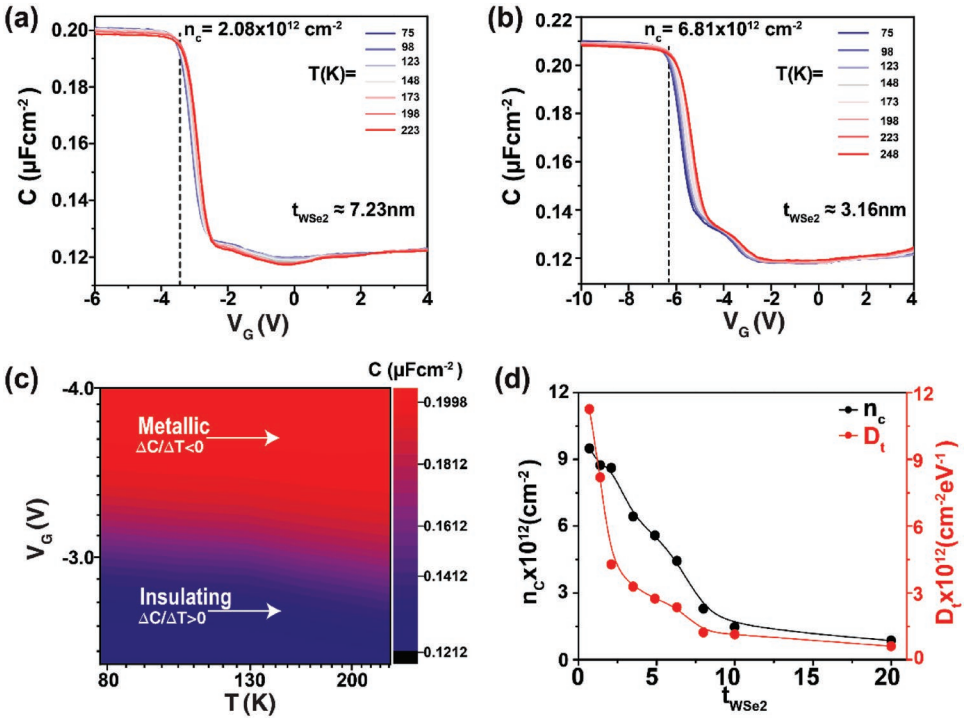

Figure 2. Metal–insulator transition driven by traps. a,b) Capacitance–voltage curves of ≈7.23 nm and 3.16 nm thick WSe_2 devices measured at various temperature points, respectively, where the dotted black vertical line indicates the MIT point . c) Color-code plots of the 7.23 nm think WSe_2 device. d) Critical carrier density (n_c) and corresponding trap density (D_t) versus thickness of WSe_2 flake (t_{WSe2}).

and q is the elementary charge.[23,36] The V_{th} is estimated from the linear region of the C-V curve (see Figure S7, Supporting Information).[24,36] Interestingly, we noticed that the transition point was dependent on WSe_2 flake thickness. It shifted toward a higher V_G with reducing WSe_2 channel thickness. To further confirm this, we tried more thickness variations and plotted the estimated n_c as a function of WSe_2 (t_{WSe2}) thickness in as shown Figure 2d. Surprisingly, results showed that n_c monotonically decreased from $\approx 9.45 \times 10^{12}$ to 8.30×10^{11} cm^{-2} as t_{WSe2} increased from monolayer to ≈20 nm. This unique trend indicates a promising thickness dependent tunable MIT characteristics in WSe_2 devices. Previously, MIT observed in 2D materials has been explained by carrier-carrier interactions and considered as the fundamental origin of MIT in a 2D system.[23,24,27,28] In contrast, 2D materials-based devices are strongly influenced by localized trap charges induced at channel-gate dielectric interface and defects.[8,9] Both carrier-carrier interaction and large trap density coexist in 2D layered materials. Their relative strengths can be further modulated by controlling the thickness of the 2D channel. In principle, interactions increase with increasing thickness of the 2D channel while trap density decreases. To understand the fundamental origin of MIT phenomena in 2D materials both effects (carrier-carrier interaction and trap density) should be considered. Therefore, to correctly analyze the MIT phenomena in WSe_2 devices different thicknesses, we considered the impact of localized D_t including interface traps and defects near the interfaces for the aforementioned thickness range in the subsequent discussion.

We estimated localized D_t from MFC-V measurement results with different excitation frequencies (f). These different excitation frequencies can excite the charge trap states when $1/f > \tau_t$ (where τ_t is the relaxation time of localized charge traps) and contribute to the measured capacitance. Whereas when $1/f < \tau_t$, charge trap states are unable to follow high frequencies. Therefore, localized D_t can be determined by capacitances measured at low and high excitation frequencies using $D_t = \frac{1}{qA}\left[\left(\frac{1}{C_{low\,f}} - \frac{1}{C_{hBN}}\right)^{-1} - \left(\frac{1}{C_{high\,f}} - \frac{1}{C_{hBN}}\right)^{-1}\right] = \frac{C_t}{qA}$, where $C_{low\,f}$ and $C_{high\,f}$ are the capacitance at low and high excitation frequencies, respectively, C_t is the trap capacitance, and A is the area of the capacitor.[31–33] Estimated D_t values at the MIT point drastically increased from $\approx 6.02 \times 10^{11}$ to 1.13×10^{13} cm^{-2} eV^{-1} as t_{WSe2} changed from ≈20 nm to monolayer as shown in Figure 2d. These obtained results indicate that thinner flakes are more susceptible to interface disorders due to large surface-to-volume ratios[37] and higher susceptibility to immediate environment induced roughness.[38] The localized D_t in WSe_2 devices can arise due to material imperfections such as chalcogen vacancies, transition metal vacancies, anti-sites (when the transition metals occupy chalcogen vacancy), dislocation, dielectric-induced defects, device processing-induced defects, and strain induced from the substrate.[39,40] These localized D_t play a significant role in altering the transport characteristic of WSe_2 devices through hopping between localized states that could be explained by the variable-range-hopping model.[41,42] In addition, these localized D_t can smear inside the bandgap and alter the band structure as well as the doping profile in 2D semiconducting materials, resulting in electrical behavior strongly affected by these trap charges.[31,40,43] Therefore, a compromised electrical performance, such as degradation in mobility,[31,38] strong Fermi level pinning,[44] and large subthreshold swing,[6] is understandable for thinner 2D flakes as compared to thicker flakes. Similarly, the current experimental study revealed that MIT observed in WSe_2 devices was strongly dependent on WSe_2 channel thickness and corresponding WSe_2/hBN interface quality. This suggests that the physical origin of MIT observed in WSe_2 devices with different thicknesses is associated with the strength of localized D_t and interface perturbation. The impact of these interface perturbations can be increased by reducing flake thickness where large localized D_t is observed. The localized D_t can lead to generate strong potential fluctuations in the band of WSe_2 due to randomly occupied charge traps at the interfaces. Consequently, different kinds of transition mechanisms are expected for WSe_2 devices with different thicknesses depending on the influence and strength of D_t.[17,45] Further investigation of D_t effect on MIT is discussed below by analyzing electrical transport data.

2.2. Electrical Transport Measurements

The thickness-dependent MIT in WSe_2 devices was further confirmed by electrical transport measurements as shown in **Figure 3**. Conductivities ($\sigma = \left(\frac{I_D}{V_D} \times \frac{L}{W}\right)$ where L, and W are the channel length and width respectively) as a function of V_G of 7.23 nm and 4.31 nm thick WSe_2 devices at different temperatures showed well-defined crossover points at V_G of − 3.6 and − 5.4V as shown in Figures 3a,b, respectively. The MIT behavior was observed in measured devices approximately the same V_G from both C-V and transport measurements, ensuring the reliability and repeatability of the data for WSe_2 devices. Transport data for both devices also clearly indicated that σ increased with decreasing temperature when V_G is higher than − 3.6V and − 5.4V for 7.23 nm and 4.31 nm devices, respectively, showing the metallic behavior while σ showed the opposite behavior when V_G is lower than − 3.6 V and − 5.4 V for 7.23 nm and 4.31 nm devices respectively, indicating the insulating phase, as shown in the inset of Figure 3a,b. To see more clearly the critical transition point from transport measurements, we plotted temperature-dependent σ for different V_G values with corresponding n_{2D} for 7.23 nm and 4.31 nm devices as shown in Figures 3c,d, respectively. It is clearly shown that σ increased with decreasing temperature attributed to the metallic behavior when n_{2D} greater than n_c (2.08×10^{12} cm^{-2}) and corresponding localized trap density $D_t \approx 3.67 \times 10^{12}$ cm^{-2} eV^{-1} for 7.23 nm device and when $n_c \approx 5.44 \times 10^{12}$ cm^{-2} and $D_t \approx 6.72 \times 10^{12}$ cm^{-2} eV^{-1} for 4.31 nm device. In contrast, σ showed the opposite trend when n_{2D} and localized D_t were smaller than the above values for both devices.

To evaluate disorders and unavoidable scatterings induced by interface traps, field-effect mobility (μ) is an important physical parameter of the measured devices. We extracted field-effect mobility (μ) using the following equation: $\mu = \left(\frac{L}{WC_G V_D}\right)\left(\frac{dI_D}{dV_G}\right)$, where C_G are the gate capacitance per unit area measured in the accumulation region of the C–V curve. The estimated μ at the transition point (μ_c) and the corresponding localized D_t

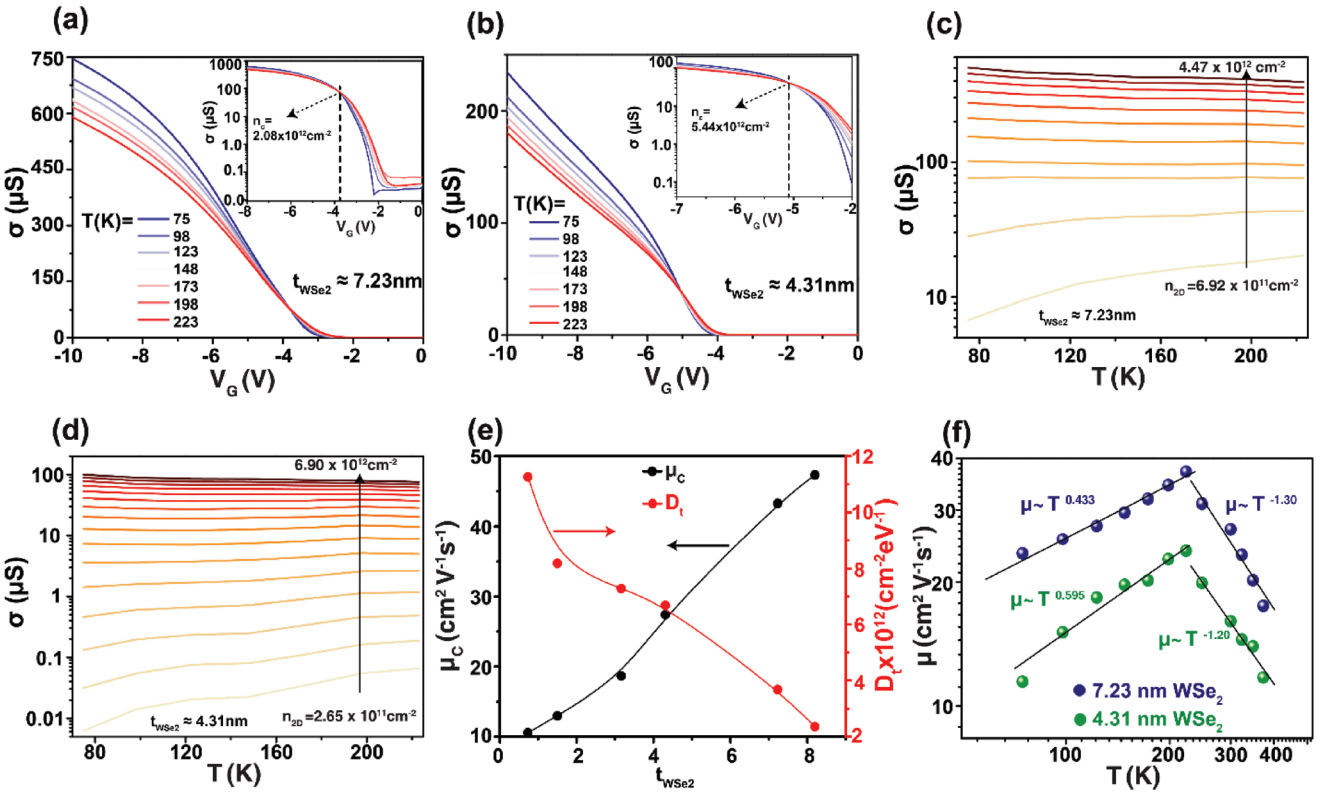

Figure 3. Thickness-dependent tunable MIT in WSe_2 devices. a,b) Conductivity versus applied gate voltage at different temperatures for ≈7.23 and 4.31 nm WSe_2 devices, respectively. Insets show conductance versus applied gate voltage in the semilogarithmic scale, where the black dotted vertical line represents transition points and arrow indicates the corresponding critical carrier densities (n_c). c,d) Conductivity versus temperature at different gate voltages, showing metallic and insulating phases of 7.23 and 4.31 nm WSe_2 devices, respectively. e) Critical mobility (μ_c) and corresponding trap density (D_t) as a function of the thickness of WSe_2 flake (t_{WSe2}) measured at 223 K. f) Mobility versus temperature for 7.23 and 4.31 nm WSe_2 devices, where solid black lines serve as guidelines for the $\mu \approx T^{-\gamma}$ relation.

as a function of respective thickness as shown in Figure 3e. They were used to determine the direct impact of localized D_t on the transport at the MIT point. The μ_c was decreased significantly from ≈47 to 11 cm^{-2} V^{-1} s^{-1} when the WSe_2 channel thickness was decreased from multilayers (≈8.2 nm) to monolayer (≈0.73 nm) while the corresponding localized D_t strongly increased from 2.35×10^{12} to 1.12×10^{13} cm^{-2} eV^{-1}. This drastic decreasing trend of μ_c was attributed to a significant increment in the localized D_t with reducing WSe_2 channel thickness. This confirms that the transport at the transition point is strongly controlled and modulated by localized D_t in the respective device, consistent with the previous reports showing the impact of substrate trap states on carrier μ in 2D materials was observed.[6,38,46]

Figure 3f shows mobility versus temperature obtained for 7.23 and 4.31 nm WSe_2 devices. Initially, μ increased until it reached a maximum value as the temperature increased from 75 to 223 K. It then decreased with the further increase of temperature. This suggests that the μ of a WSe_2 depends on different scattering mechanisms and distribution of localized D_t. Theoretically, mobility is determined by intrinsic electron-phonon coupling at higher temperatures, often known as phonon limited μ. However, experimentally observed μ values are predominately limited by several external factors such as defects, Coulomb impurities, and localized D_t at the channel-gate dielectric interface as a major factor.[23,38,47] In addition, we fitted results of μ versus temperature to the relation of, $\mu \approx T^{-\gamma}$, where γ is the critical exponent that depends on scattering. The fitted value of γ is − 1.30 for 7.23 nm and − 1.20 for 4.31 nm devices at temperatures greater than 223 K, suggesting that the electron scattering is due to optical phonons. For temperatures lower than 223 K, the fitted value of γ is 0.433 for 7.23 nm and 0.595 for 4.31 nm, indicating the presence of charge impurity scattering at the interface.

The occurrence of MIT in 2D semiconductors can be further confirmed by the Ioffe–Regel criterion.[11,23,48] According to this criterion, the MIT can be observed in the system when parameters $k_F l \approx 1$. The system would be at the metallic phase for $k_F l >> 1$ whereas the system considered an insulator when $k_F l << 1$. Here, $k_F = \sqrt{2\pi n_{2D}}$ is the Fermi wave vector and $l = \frac{\hbar k_F \sigma}{n_{2D} q^2}$ is the mean free path of the carrier. The estimated $k_F l \approx 1.65$ was obtained at transition point of $V_G = -3.6$V for 7.23 nm WSe_2 device, showing a good agreement with the loffe–Regel theory. Our other measured WSe_2 devices also exhibit $k_F l$ close to 1.6, values in different regions (insulating, near MIT point and metallic,) for different thicknesses are given in Supporting Information S8 and Tables S1–S3 (Supporting Information). In addition, we estimated the Fermi temperature (i.e., $T_F = \frac{\pi \hbar^2 n_c}{k_B m^*}$)

at the MIT point for different thickness devices using the value of n_c given in Figure 2d. Here, m^* is the effective mass, k_B is the Boltzmann constant, and ħ is the Plank constant. We obtained Fermi temperatures in the range of ≈69 to 773 K for different thickness WSe_2 devices using the respective n_c from 8.30×10^{11} to 9.45×10^{12} cm^{-2} and considering $m^* = 0.34\ m_o$.[49] Further details are given in Supporting Information S9 and Table S4 (Supporting Information). Previously, Fermi temperature from 56 to 556 K in a few layers ReS_2 has been reported.[27] The slightly large value of T_F obtained in this study is due to different values of m^* and n_c for different thicknesses.

2.3. Thickness-Dependent Percolation Critical Behavior

According to the scaling theory of localization, a carrier-carrier interaction in the system can be determined by the strength of Coulomb interaction between carriers. In the presence of localized D_t, the strength of Coulomb interaction is characterized by the Wigner-Seitz radius (r_s), defined as the ratio of potential (coulomb, E_C), and kinetic (Fermi, E_F) energy by $r_s = \frac{E_C}{E_F} = \frac{n_v}{a^*\sqrt{\pi n_{2D}}} = \frac{m^* e^2 n_v}{4\pi\varepsilon\hbar^2\sqrt{\pi n_{2D}}}$, where n_v represents the number of degenerate valleys, $a^*=4\pi\varepsilon\hbar^2/m^*e^2$ is the effective Bohr radius, and ε is the dielectric constant of the material.[23] A system can be considered strongly interacting if the $r_s>>1$.[50] Therefore, we calculated values of r_s at the transition point for WSe_2 devices with different thicknesses to figure out the variation in interaction strength depending on flake thickness. Estimated values of r_s at MIT point ranged from ≈8.60 to 2.20 as the thickness decreased from ≈8.2 nm to 0.73 nm (monolayer) considering thickness dependent m^* and ε reported by Wickramaratne et al. and Jeon et al., respectively.[49,51] The decreased Coulomb interaction is due to the increasesd D_t and n_c and decreased m^* and ε with decreasing flake thickness. Estimated values of r_s at MIT point for WSe_2 devices with different thicknesses is slightly different from those previously reported in the case of MoS_2 due to relatively high m^* and different ε of MoS_2.[23] The significantly decreased value of r_s clearly indicates that the Coulomb interaction between carriers becomes weaker with reducing flake thickness. Consequently, the strength of the localized D_t governs the system. In the presence of high localized D_t, the MIT in different 2D systems can be analyzed by the percolation model of conductivity.[26,30,52] Therefore, we analyzed the percolation model of conductivity for all measured devices having different thicknesses of WSe_2 flakes to provide further insight into the thickness-dependent tunable MIT in WSe_2 devices.

The conductivity in percolation driven transition is expressed by a power law to carrier density by $\sigma\ (n) = A(n - n_{cp})^{\delta}$, where A, δ and n_{cp} are the constant of proportionality, critical percolation exponent, and critical carrier density respectively.[24,53] Measured σ values of multilayers (7.23 nm), few layers (3.16 nm), and monolayer (0.73 nm) WSe_2 devices are given in **Figure 4**a. Based on power-law fitting, δ values of 1.377 ± 0.013 to 1.4257 ± 0.022 for monolayer (0.73 nm) and 1.743 ± 0.057 to 1.966 ± 0.052 for few-layer (3.16 nm) were obtained within the measured temperature range of 75 to 300 K, close to the 2D percolation exponent value of 1.33. [30,52,53] Obtained values of δ from the fitting of power-law at different temperatures for

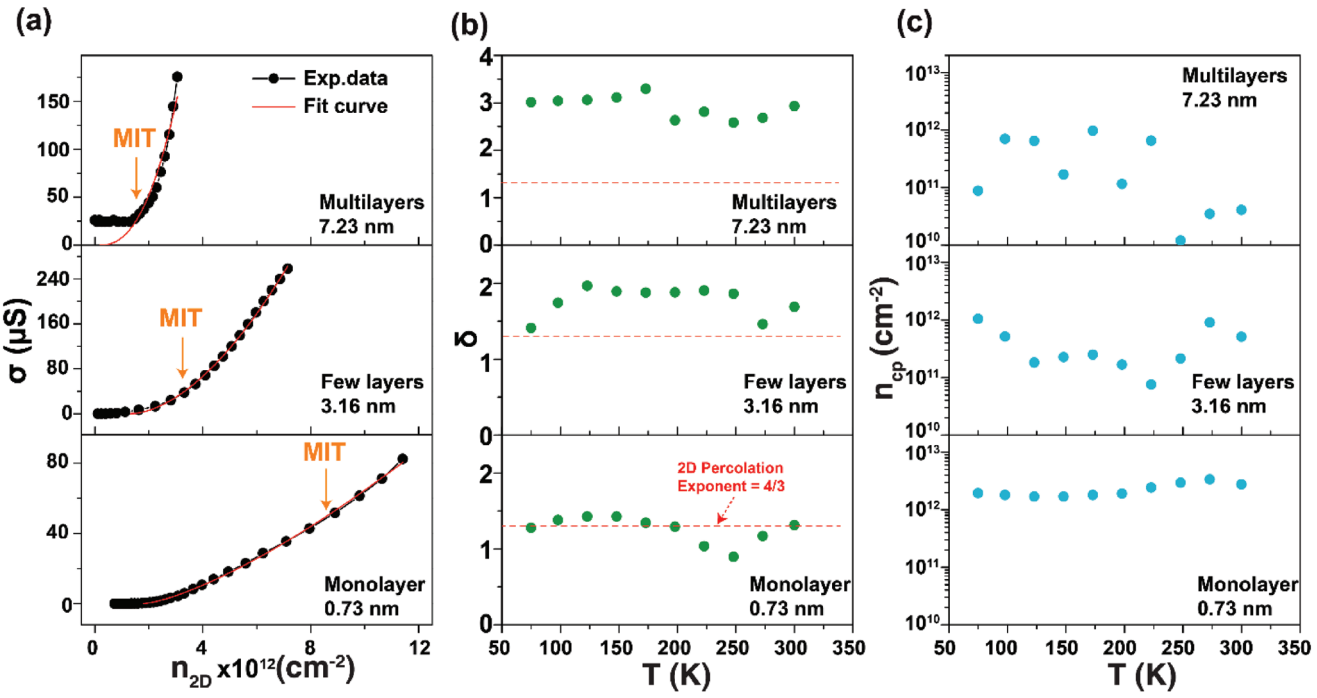

Figure 4. Thickness-dependent percolation analysis. a) The fitting of measured conductivity as a function of carrier density for multilayer (7.23 nm), few-layer (3.16 nm), and monolayer (0.73 nm) WSe_2 devices was performed using the percolation model of $\sigma\ (n) = A(n - n_{cp})^{\delta}$. The orange arrow in the vertical direction represents the position of MITs. b,c) Variation of critical percolation exponents (δ) and critical carrier density obtained by percolation fitting for different thickness devices. The dotted red lines in (b) represent expected values of δ in the 2D material system.

devices with different thicknesses are shown in Figures 4b. We found an excellent agreement between the measured conductivity data and the theoretical model for WSe_2 devices when WSe_2 flakes were used up to a few layers. Therefore, we believe that the MIT observed in WSe_2 devices using up to a few layers of WSe_2 flake is due to charge density inhomogeneity caused by potential fluctuation induced by localized D_t which leads to a percolation-driven transition. However, in the case of multilayer WSe_2 devices, value of δ were 2.586 ± 1.366 to 3.293 ± 1.701, indicating that the percolation theory is no longer valid in the multilayer WSe_2 system and that the transition is likely to be led by carrier-carrier interactions. Such deviations with increasing the thickness of WSe_2 flakes indicate that the nature of the transition strongly depends on the relative strength of localized D_t and carrier-carrier interactions depending on the thickness of WSe_2 flakes and interface perturbation. In addition, it is important to point out that the value of n_{cp} extracted from the theoretical model is lower than the corresponding estimated value of n_c at the MIT cross-over point from experimental data for all devices. Estimated n_{cp} values at different temperatures for different device thicknesses are shown in Figure 4c. At 75K, n_{cp} was $\approx 8.84 \times 10^{10}$ cm^{-2} and n_c was$\approx 2.08 \times 10^{12}$ cm^{-2} for 7.23 nm (multilayer) device, n_{cp} was $\approx 1.3 \times 10^{12}$ cm^{-2} and, n_c was $\approx 6.81 \times 10^{12}$ cm^{-2} for 3.16 nm (few layers) device, while n_{cp} was $\approx 1.9 \times 10^{12}$ cm^{-2} and n_c was $\approx 9.45 \times 10^{12}$ cm^{-2} for the monolayer device. The difference in critical carrier density between theoretical and experimental data is due to thermal activation of localized states and hopping conductivity at finite temperature.[28]

Findings of this study suggest that disorders induced by localized traps at interfaces and carrier–carrier interactions are both important parameters to analyze MIT in WSe_2 devices depending on the thickness of the WSe_2 flake. Because the thickness of the 2D flake primarily determines the relative strength of disorders and carrier-carrier interactions in the system, it controls the transition mechanism in a 2D layered system. We plotted D_t and r_s obtained at MIT point as a function of t_{WSe2} as shown in **Figure 5**a. When the WSe_2 channel thickness was downsized from few-layers to a monolayer (light yellow shaded area in Figure 5a) disorders might have prevailed over the carrier–carrier interactions, leading to a disorder-dominated transition. In contrast, the transition observed in multilayer WSe_2 devices was possibly interaction dominated as evidenced by the large value of Coulomb interaction shown in the light green shaded area in Figure 5a. Lastly, to qualitatively understand the formation of random potential fluctuations from localized trapped charges at the WSe_2/hBN interface, a comprehensive energy band diagram is driven for WSe_2 as shown in Figure 5b. In thinner WSe_2 devices below a few-layers where percolation theory is obeyed, disorder-induced localized D_t and screening in a device play a significant role. High localized D_t values in thinner devices can lead to large interface perturbations and high inhomogeneous electronic potential landscape which can effectively control the transport behavior of the device. In addition, the screening of these trapped charges becomes weaker due to the large bandgap of WSe_2, unlike at graphene system.[45] With increasing flake thickness the localized D_t decreases and screening of these trapped charges can be increased. Consequently, less potential fluctuation in the band of WSe_2 is expected.

3. Conclusion

We performed a detailed analysis of thickness-dependent MIT in WSe_2 devices by varying the WSe_2 channel thickness from 20 to 0.73 nm (monolayer). We observed that MIT in WSe_2 devices was strongly dependent on channel thickness and the corresponding localized D_t at the WSe_2/hBN interface. The estimated critical carrier density (n_c) at the transition point significantly increased with the decreasing thickness of WSe_2 flakes, attributed to dramatically increased localized D_t in thinner devices. Furthermore, we found an excellent agreement between experimentally measured conductivity data and theoretical percolation model for WSe_2 devices with WSe_2 flakes having thickness up to a few-layers. This suggests that the percolation type MIT is the dominant mechanism in thinner WSe_2 devices due to the random potential fluctuation caused by large localized D_t at the interface. In contrast, the percolation theory is no longer valid in multilayer WSe_2 devices as the transition is likely driven by carrier-carrier interactions. This is also confirmed by the large strength of Coulomb interaction estimated by the Wigner–Seitz radius. These findings indicate that tunable MIT with the thickness of flake in layered WSe_2 would be a strong candidate for engineering phase change-based devices such as non-volatile

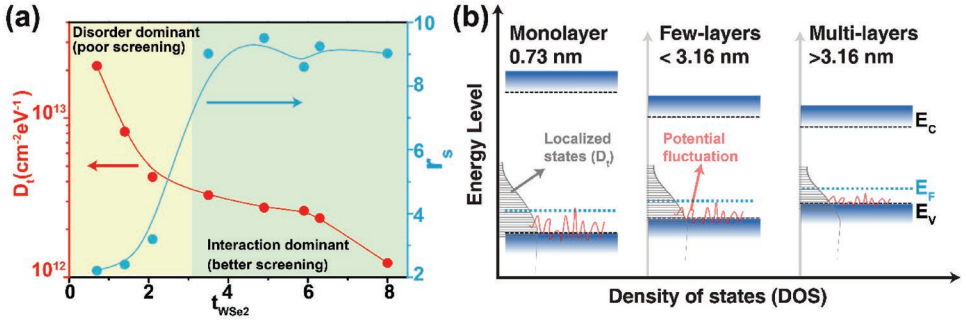

Figure 5. Summary of transition mechanism. a) Variation of trap density (D_t) and Wigner–Seitz radius (r_s) estimated at MIT point for WSe_2 devices with different thicknesses. The light-yellow shaded area represents localized trap dominated region (below few layers of WSe_2) light green area represents multilayers where interaction is the dominant mechanism of transition. b) Schematic to illustrate the distribution of localized D_t with corresponding possible random potential fluctuation WSe_2 devices with different thickness.

memory devices as it can be used to control and tune the transition point by controlling the thickness of flakes.

4. Experimental Section

Device Fabrication: A van der Waals bottom contact field-effect transistor (FET) was fabricated, as shown in Figures 1a,b. First, to deposit bottom electrodes, a pre-pattern was designed on a p-Si/SiO_2 substrate by standard electron-beam lithography, and 5/25 nm thick Cr/Pt metal electrodes were deposited by electron-beam evaporation under high vacuum (8×10^{-8} Torr) to ensure good electrical contacts. The mechanically exfoliated WSe_2 from bulk ≈20 nm thick to monolayer was picked with a 20 nm thick hBN flake and transferred onto the pre-patterned electrode with a dry transfer method using an auto-transfer stage inside a glove box with moisture and oxygen concentration < 1 ppm, which enabled to avoid the formation of bubbles and chemical residues at the WSe_2/hBN interface. Finally, the top gate Cr/Au metal electrode of 5/70 nm thickness was deposited to complete the device fabrication.

Device Characterization: After completing the fabrication process, electrical (current-voltage and capacitance-voltage) measurements were conducted using a semiconductor parameter analyzer (Agilent 4155C) and an LCR meter (Agilent E4980A) in a vacuum chamber with varying temperatures from 300 to 75 K.

Atomic Force Microscopy (AFM). All the AFM analyses were performed at room temperature under atmospheric pressure by placing the sample on a metal puck that was grounded.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

capacitance–voltage (C—V), low-temperature measurement, transport (I—V) measurements, trap density (D_t), tunable metal-insulator transition (MIT), WSe_2 thicknesses

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