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Low-resistance metal contacts to encapsulated semiconductor monolayers with long transfer length

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Two-dimensional semiconductors such as transition metal dichalcogenides are of potential use in electronic and optoelectronic devices due to their high mobility, direct optical bandgap and mechanical flexibility. These semiconductors are often encapsulated with hexagonal boron nitride to minimize extrinsic disorder and improve performance, but it is challenging to make high-quality contacts to encapsulated high-purity monolayers. Here we show that metal contacts embedded within hexagonal boron nitride can be transferred onto clean transition metal dichalcogenide monolayers, in an approach that reduces doping, strain and interfacial roughness compared with evaporated metal contacts. Contacts to encapsulated ultraclean tungsten diselenide monolayers created using this technique exhibit a room-temperature contact resistance of around 5 kΩ μm, and provide transistors with zero hysteresis and room-temperature mobility of 655 $cm^2 V^{-1} s^{-1}$. The contacts also exhibit a transfer length of 1 μm, which is several orders of magnitude larger than the channel thickness.

Atomically thin semiconductors such as transition metal dichalcogenides (TMDs) are of interest in the development of electronic and optoelectronic devices due to their high performance and novel properties, particularly at the monolayer level[1–4]. For many applications, it is necessary that devices have ultrapure TMD materials with low intrinsic defects, encapsulation that minimizes extrinsic disorder and high-quality electrical contacts to connect these materials with external circuits[5–9]. Substantial progress in all three of these areas has recently been made. Semiconducting TMD crystals, including tungsten diselenide (WSe_2) and molybdenum diselenide ($MoSe_2$), that are synthesized with a self-flux technique can offer reduced defect density compared with materials grown with chemical vapour transport (CVT)[10], and monolayers of these crystals exhibit quantum phenomena such as fractional quantum Hall states[10,11]. Hexagonal boron nitride (hBN) is a low-disorder insulating material that can be used for encapsulation, and hBN-encapsulated TMDs have been shown to offer improved electronic and optical properties[12,13]. Finally, various techniques have been developed to create ohmic contacts to semiconducting TMDs, including using low-work-function metals or hybrid metal–hBN layers, graphene with tuned Fermi levels, mechanically transferred metals, and low-melting-point metals such as indium and semimetallic bismuth[14–20].

However, it remains difficult to achieve high-quality contacts to ultrapure TMD monolayers with hBN encapsulation. Previous approaches typically yield only n-type contacts and perform poorly when made with high-purity semiconducting TMDs because of the absence of intrinsic defects that can be used to dope the material. Lithography and metal evaporation processes can also damage the TMD layer, particularly when it is a monolayer. Mechanical transfer of contacts onto TMDs avoids this and has proven successful for multilayers[16,17,20]. Transferred via contacts (TVCs) combine mechanical transfer and hBN encapsulation by incorporating metal electrodes into holes etched into hBN crystals. This approach can provide simultaneous electrical contact and encapsulation for air-sensitive two-dimensional (2D) metals[20], and has been used to create contacts to 2D semiconductors such as multilayer WSe_2 (ref. [17]). However, ohmic contacts were achieved only for CVT-grown WSe_2 with high defect density, and the assembly process showed low yield and low performance for monolayers (Supplementary Fig. 1)[17]. TVCs do not work for quasi-intrinsic semiconducting TMDs of any thickness and have yielded only n-type transistors when high-work-function electrodes (such as platinum (Pt)) were used, indicating non-ideal band alignment at the interface[17].

In this Article, we identify key factors that influence contact quality for monolayer TMDs—including mechanical strain at the interface, flatness and surface cleanliness underneath the contacts—and then report a three-step assembly procedure to control these effects and create doping-free electrical contacts. Our approach uses a flipped-assembly step with a polymer-supported hBN layer to reduce heterogeneous strain when transferring the TMD; a transferring-after-etching step in which the top hBN layer is etched and then transferred before depositing metal into the gaps, to ensure a clean and flat interface between the hBN and metal; and a strain-free assembly step to fabricate metal–hBN and TMD–hBN structures, and create the final heterostructure. We use the approach to make contacts between Pt embedded within hBN and quasi-intrinsic monolayer WSe_2 on hBN. The resulting hBN-encapsulated WSe_2 devices exhibit almost no strain and excellent electrical performance, behaving as p-type transistors with zero hysteresis, contact resistance R_c of 5 kΩ μm and room-temperature mobility of 655 $cm^2 V^{-1} s^{-1}$. Contact-end measurements show that the contacts have a transfer length of 1 μm, placing them in a different regime from conventional bulk materials and most previously

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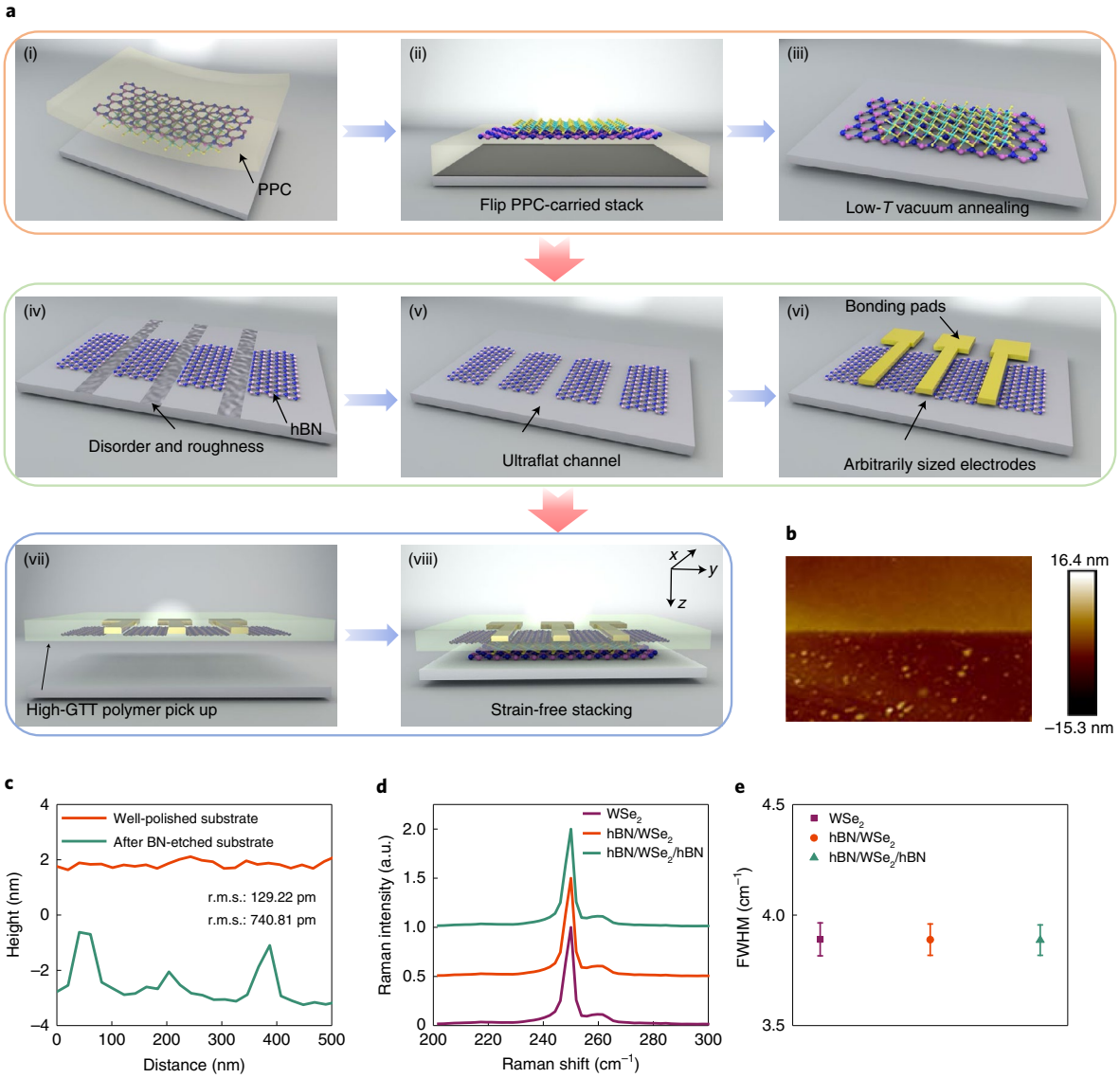

Fig. 1 | Assembly and characterization of 3D metal electrodes–hBN/monolayer TMDs/hBN heterostructure. a, Flipped assembly of hBN/WSe_2: layer-by-layer picking up of hBN and WSe_2 (i); flipping the PPC to expose the monolayer TMDs upward (ii); annealed in a vacuum to remove the underneath PPC (iii). Etching of hBN and electrode deposition: etching hBN (iv); transferring the etched hBN onto a well-polished silicon wafer (v); fabricating arbitrarily sized electrodes (vi). Heterostructure assembly: detaching the prepared metal–hBN hybrid heterostructure (vii); GTT, glass-transition temperature; strain-free lamination process (viii). **b**,**c**, AFM images of the etched (bottom) and unetched (top) SiO_2 (**b**) and the AFM profile (**c**). **d**, Raman characterization of the monolayer WSe_2 before and after assembly into the heterostructure. **e**, FWHM and error bars of the Raman spectra in **d** were extracted using Lorentz fit. Error bars fall into the range of $\pm 0.08\,cm^{-1}$.

studied 2D materials. We attribute this to the lack of doping or damage at the contacts, low number of defects in the TMD crystal and high resistivity to charge injection across the van der Waals gap.

Assembling metal–hBN/monolayer TMDs/hBN heterostructures

The typical method used for the fabrication of TVCs is to etch holes in an hBN flake, evaporate metal into the holes, pick up the metal–hBN structure, use the metal–hBN to pick up a 2D flake and drop the stack onto a second hBN flake. Supplementary Fig. 1 illustrates two major factors affecting the quality and reliability of contacts fabricated in this way. First, when the hBN is etched to form the through vias, the substrate underneath can be partially etched, roughened and contaminated with adsorbates (Fig. 1b and Supplementary Fig. 1a, steps (i)–(iii)). When metal contacts are evaporated in the same location, they can slightly protrude from the hBN, and 'inherit' roughness and contamination from the substrate. This may explain why, despite being air stable, WSe_2 requires strict in-glovebox assembly and devices that are assembled in air showed high contact resistance regardless of the WSe_2 layer thickness[17]. Second, the typical pick-up and drop-down process involves large strain (Supplementary Fig. 1a, steps (iv)–(vi)). This can lead to shifting of the metal electrodes outside the hBN holes, as well as cracking of the TMDs and hBN (Supplementary Fig. 1b). Specifically, when the metal contacts are not perfectly planar with the hBN, strain can cause cracking of the encapsulated TMDs at the edges of the contacts. More importantly, deformation of the capping polymer during the dropping-down process leads to substantial distortion, which further induces strain on the layers underneath. These are probably the reasons

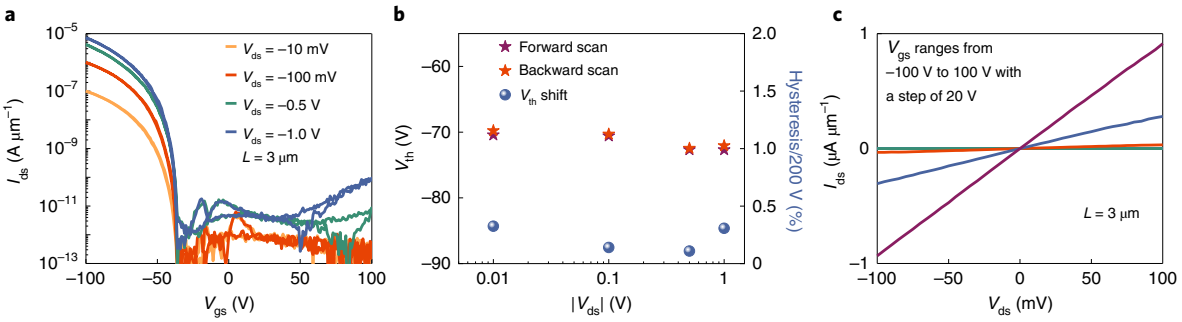

Fig. 2 | Room-temperature electrical performance of monolayer WSe_2 FET. a, Transfer characteristics at different drain–source biases. **b**, Measured threshold voltage and hysteresis characteristics. **c**, Output characteristics at low drain–source bias.

for the observed low yield for monolayers, which are the most susceptible to fracture.

To mitigate these effects, we implemented a process that provides very clean and flat contacts that are planar with the hBN layer, and minimizes strain during assembly. This process consists of three main steps (Fig. 1a). First, flipped assembly is described (Fig. 1a(i)–(iii)): rather than picking up the semiconducting TMD with the top hBN, we pick it up with a polymer-supported hBN flake and place the whole structure upside down on the target wafer (Supplementary Fig. 2a shows the polymer slides). Heating under a vacuum removes the polymer film, leaving the polymer-free TMD on top of the bottom hBN flake (Supplementary Fig. 3 shows the atomic force microscopy (AFM) characterization of a flipped monolayer WSe_2/hBN structure after vacuum annealing)[21]. This process reduces the heterogeneous strain that can arise when the TMD is picked up by an hBN–metal composite layer. As shown in Fig. 1d, the Raman peaks of WSe_2 are maintained at the same position of around 250 cm^{-1} before and after stacking, indicating that no extra strain was introduced during this stacking process.

Second, Fig. 1a(iv)–(vi) shows the transferring-after-etching process: we etch the top hBN flake into parallel strips and transfer them to a well-polished silicon substrate. A series of Pt/Au electrodes, including contacts and testing pads, are then deposited into the gaps, slightly overlapping the hBN strips. Transferring the hBN before evaporation ensures that the bottom surface of the metal is clean, smooth and completely planar with the hBN layer. The improved substrate flatness is shown in the AFM image and profile (Fig. 1b,c).

Last, Fig. 1a(vii)–(viii) shows the strain-free assembly: we pick up the metal–hBN structure and transfer it on top of the prepared TMD–hBN heterostructure in a way that minimizes shear motion during the assembly process. To achieve this, we used hard-cured polydimethylsiloxane (PDMS) with a poly(methyl methacrylate) (PMMA) capping layer (Supplementary Fig. 2b). When picking up the metal–hBN hybrid structure, we peel the structure in the direction parallel to the metal strips, minimizing strain at the metal–hBN interface (Supplementary Fig. 4). The drop-down procedure (Fig. 1a(viii)) is performed at 80 °C, well below the PMMA glass-transition temperature (http://polymerdatabase.com/polymer%20classes/Polymethacrylate%20type.html#:~:text=Most%20commercial%20grades%20of%20PMMA,87%20to%20157%20%C2%B0C) of 125 °C. This, together with the stiffness of the PDMS layer, ensures that the top layer stays relatively rigid during the process, with a large bending radius close to infinity that minimizes lateral strain[22]. Thus, monolayer WSe_2 was naturally sealed and was placed near the neutral mechanical plane. To quantify the shear-motion-induced strain, we employed a model developed elsewhere[23] to analyse the deformation of monolayer TMDs induced by relative shear motion. The undesired displacement could be reduced to a negligible level by minimizing the horizontal shift (Supplementary Section 5). It is noted that additional large-scale metal features can be included in the same metal layer as the contact electrodes, allowing us to encapsulate/contact the monolayer TMDs and deposit bonding pads in a single step, further reducing the potential sources of contamination. As shown in Fig. 1d,e, the Raman spectra showed the same peak positions and full-width at half-maximum (FWHM) before and after heterostructure assembly, indicating that the assembly process does not introduce appreciable strain or doping[24].

Electrical characterization of the monolayer WSe_2 transistor

To investigate whether strain-free assembling yielded improved device performance, we assembled devices using monolayer WSe_2 exfoliated from crystals with defect density below 10^{10} cm^{-2}. For comparison, this is 2–3 orders of magnitude lower density than found in typical commercially CVT-grown crystals[10] (Supplementary Section 6 and Supplementary Fig. 6a–c). Supplementary Fig. 6d shows the photoluminescence measurements of the monolayer. These devices were characterized as field-effect transistors (FETs), with the silicon wafer acting as a back gate and 285 nm SiO_2 (plus the bottom hBN, typically ~30 nm thick) as a gate dielectric.

Figure 2a shows the room-temperature transfer curves for device D1 with a channel length of 3 μm. The drain–source current (I_{ds}) turns on strongly below a gate–source bias of $V_{gs} = -40$ V, and weakly above $V_{gs} = 50$ V with a large drain–source bias of $V_{ds} = -1$ V. The nearly symmetric positions of the p-branch and n-branch conduction indicate that the channel is close to intrinsic (undoped), consistent with characterization by scanning tunnelling spectroscopy (Supplementary Fig. 6c); the larger current at negative V_{gs} is consistent with efficient hole injection from the high-work-function Pt. For the p branch, we find a threshold voltage V_{th} of −70 V, obtained using a linear extrapolation method (Supplementary Fig. 7). At $V_{ds} = -1$ V, the device shows an on-state current of 7.4 μA μm^{-1} at $V_{gs} = -100$ V (ref. [25]) and an on/off ratio of 10^8. In addition, the device shows low hysteresis (<0.5%) when the gate voltage (V_{gs}) is scanned forward and backward over the range of −100 to 100 V (Fig. 2b). The output characteristics (Fig. 2c) show linear I_{ds}–V_{ds} behaviour, consistent with ohmic contacts.

To independently measure the channel and contact resistance, we performed transfer length method (TLM) measurements for a series of devices (D2; Supplementary Fig. 8 shows the images of D2) using the configuration shown in Fig. 3a (ref. [25]). First, we measured the transfer characteristics (Supplementary Fig. 9 shows the corresponding output characteristics) between contacts A and D at small $V_{ds} = -0.01$ V (Fig. 3b), from which we could extract the transconductance at various V_{gs} values. The sheet carrier density was assumed to be the gate capacitance, that is, $C_b = \varepsilon_b/t_b$, multiplied by the overdriven voltage, namely, $Q = C_b \times (V_{gs} - V_{th})/q$, where q is the elementary charge and V_{th} is the threshold voltage (Supplementary Section 10 shows the characterization of SiO_2 thickness and

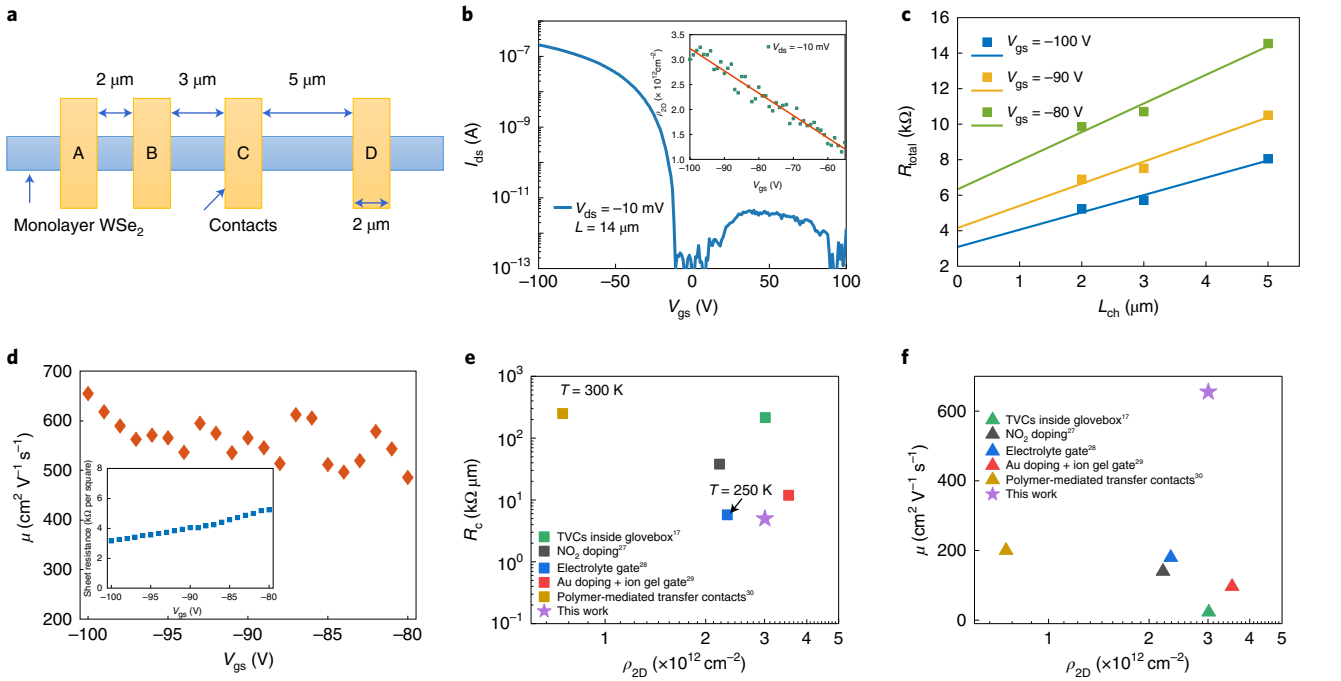

Fig. 3 | Characterization of contact resistance and mobility. a, Schematic of the TLM measurement configuration. **b**, Transfer characteristics at low drain-source bias. The inset shows the carrier density extracted as a function of V_{gs}. **c**, Plot of total resistance as a function of channel length to obtain the sheet resistance of the channel and contact resistance values. **d**, Extracted conductivity mobility. The inset shows the sheet resistance. **e**,**f**, Comparison of R_c (**e**) and mobility (**f**) with previously reported values for monolayer WSe_2.

gate capacitance). As indicated in Fig. 3b (inset), the hole density reached about $3\times10^{12}\,cm^{-2}$ at $V_{gs}=-100\,V$. At this point, the extracted two-probe field-effect hole mobility was $618\,cm^2\,V^{-1}\,s^{-1}$. In the on state, at $V_{gs}=-100\,V$, we extracted R_c and R_{sh} as $\sim5\,k\Omega\,\mu m$ and $\sim3.2\,k\Omega$ per square, respectively (Fig. 3c). The conductivity mobility ($\mu_c=1/(neR_{sh})$) was also extracted with the highest value of $655\,cm^2\,V^{-1}\,s^{-1}$ at the same V_{gs} of $-100\,V$. The values of R_c and R_{sh} can be used to estimate the properties of the device with a specific channel length. For instance, the FET's mobility is $\sim400\,cm^2\,V^{-1}\,s^{-1}$ for a $5\,\mu m$ device but drops to $\sim160\,cm^2\,V^{-1}\,s^{-1}$ for $1\,\mu m$ channel length. In the short-channel limit, the on current is limited by contact resistance ($2R_c\approx10\,k\Omega\,\mu m$) and will thus reach $\sim100\,\mu A\,\mu m^{-1}$ for $V_{ds}=-1\,V$ in principle.

To verify the device fabrication reliability, we fabricated another group of devices (D3). These exhibited similar performance as that achieved for D2 (Supplementary Fig. 11). We also created devices using monolayer WSe_2 derived from a crystal grown by CVT with defect density of the order of $10^{13}\,cm^{-2}$ (Supplementary Fig. 6b). These showed contact-dominated behaviour with resistance above $100\,k\Omega$ (Supplementary Fig. 12). This higher contact resistance may be due to Fermi-level pinning by the defects. Finally, we fabricated devices with flux-grown monolayers in which Pt contacts were deposited by evaporation. These exhibited resistances of over $200\,M\Omega$ (Supplementary Fig. 13).

Figure 3e,f benchmarks the performance of these devices against other reported values using various fabrication methods. Here we restrict the comparison with studies of p-type contacts to monolayer WSe_2. Figure 3e shows the room-temperature contact resistance as a function of carrier density. To the best of our knowledge, the contact resistance value is among the lowest reported in the literature so far[17,26–29]. For instance, metal contacts with electrolyte gate doping have larger contact resistance even at a higher carrier density of $\sim3.5\times10^{12}\,cm^{-2}$ (ref. [27]). Figure 3f shows the mobility versus carrier density. The mobility exceeds that obtained by other methods such as transferred metal contacts embedded in polymer[29] and previously described TVCs (Supplementary Section 10)[17]. The monolayer WSe_2 p-FET performance is comparable with the best values achieved for n-type FETs with monolayer MoS_2 (ref. [19]), indicating the potential to create monolayer semiconducting TMD-based complementary metal–oxide–semiconductor architecture.

Probing the mechanism underlying low contact resistance

The previous measurements demonstrate that the low contact resistance to high-purity monolayer WSe_2 can be achieved using an assembly process that minimizes doping and strain. To better understand the nature of these contacts, we used a standard technique that models the contact as a resistor network with contact resistivity ρ_c and sheet resistance R_{sk}, connected to the channel with sheet resistance R_{sh} (Fig. 4a). The transfer length $L_t=\sqrt{\rho_c/R_{sk}}$ determines the length scale for current flowing from the channel to the contact. These parameters can be independently determined by a combination of TLM measurements performed above and contact-end resistance measurements (Fig. 4b and Supplementary Fig. 14). An analysis of the resistor network shows that the contact front resistance (R_{cf}) is given by

$$R_{cf}=\frac{\rho_c}{L_tW}\coth\left(L/L_t\right), \quad (1)$$

where L is the contact length and W is the channel width. Usually, R_{cf} is referred to simply as the contact resistance R_c, and has been derived from the TLM measurements. The network analysis also yields the contact-end resistance (R_{ce}), given by the ratio of voltage at the far end of the contact ($x=L$) to the applied current:

$$R_{ce}=\frac{\rho_c}{L_tW}\frac{1}{\sinh(L/L_t)}. \quad (2)$$

To determine R_{ce}, we used the extra resistance measurement technique[30], where R_{ce} is given by $R_{ce}=\frac{1}{2}(R_{12}+R_{23}-R_{13})$,

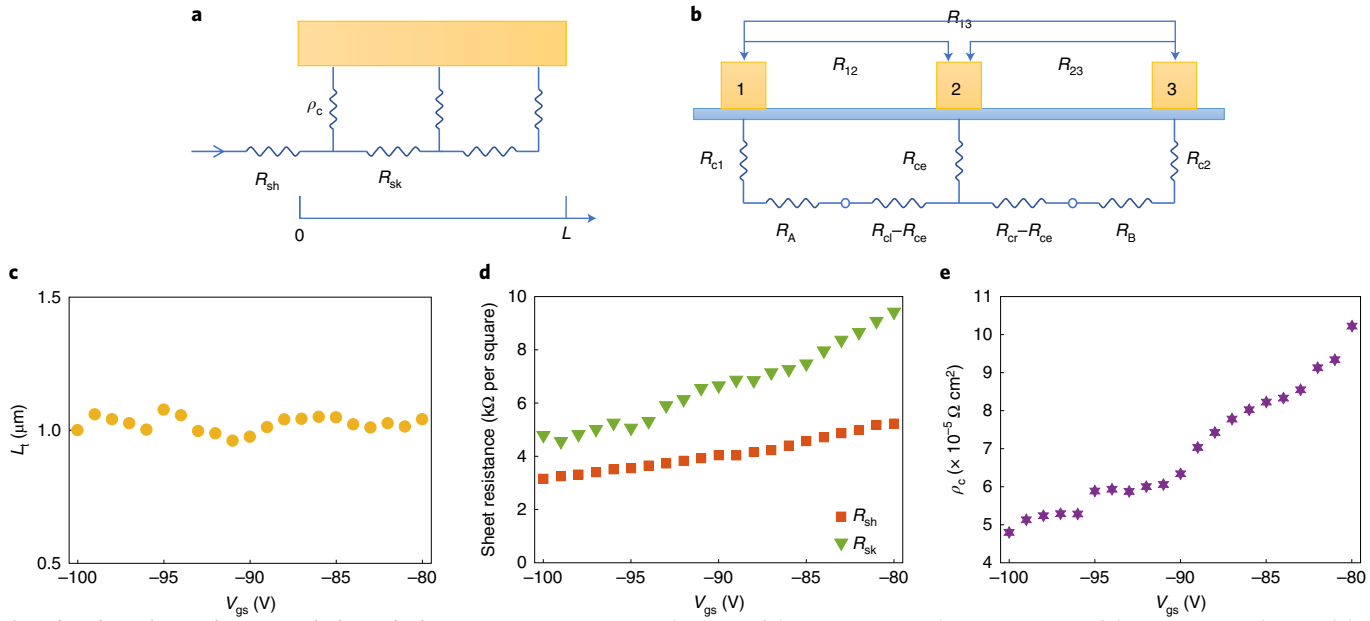

Fig. 4 | Probing the mechanism underlying the low contact resistance. a, Schematic of the resistor network representation of the transmission line model. **b**, Extra resistance measurement method used to derive contact-end resistance. **c**–**e**, Transfer length (L_t), sheet resistance in the channel (R_{sh}) and beneath contacts (R_{sk}), and contact resistivity (ρ_c) as a function of V_{gs}.

where the configurations for R_{12}, R_{23} and R_{13} are shown in Fig. 4b. Supplementary Fig. 15 shows the experimental R_{cf} and R_{ce} as a function of V_{bg}.

Also, L_t can then be determined from the ratio of the measured R_{cf} and R_{ce}:

$$\frac{R_{cf}}{R_{ce}} = \cosh(L/L_t). \quad (3)$$

Finally, the derived value of L_t can be used to determine ρ_c and R_{sk}.

Figure 4c–e shows the derived values of L_t, R_{sk} and ρ_c in the on state ($-100 < V_{bg} < -80$ V). Over this range, L_t is found to be roughly 1 μm. Here R_{sk} varies from roughly 4 to 10 kΩ per square, and is within a factor of two of the value of R_{sh} extracted using the TLM measurement. This indicates that Pt electrodes minimally perturb the underlying WSe_2 through either strain or doping. In fact, close alignment between the Pt Fermi level and valence-band edge of the WSe_2 monolayer is predicted by density functional theory calculations[31]. Finally, ρ_c falls within the range of ~$5–10 \times 10^{-5}$ Ω cm².

Figure 5 compares the values of L_t against ρ_c for these devices with both conventional FETs and previous studies of evaporated metal contacts to TMDs (although there are many studies of contacts to TMDs, only a few have rigorously measured these values)[32–35]. On this plot, contours of constant $R_{sk} = \rho_c/L_t^2$ and $R_{cf} = \rho_c/L_t$ (in the limit $L \gg L_t$) are indicated by the lines shown. Notably, all the top contacts to TMDs show ρ_c that is 3–4 orders of magnitude larger than is achieved for bulk semiconductors. This highlights the challenge posed by the large van der Waals gap between the metal and TMD. Conventional evaporated contacts to TMDs also show large values of R_{sk}, presumably due to damage from the evaporation process, which further increases R_{cf}. Doping can reduce both ρ_c and R_{sk}, as shown by a recent study[35] of six-layer WSe_2. In the devices studied here, the smaller value of R_{cf} is achieved not by doping the contacts but by avoiding damage such that R_{sk} is minimized and L_t is extremely long.

In conventional FETs, low-resistance contacts are achieved by the local doping of contact areas and using silicon-based metal alloys.

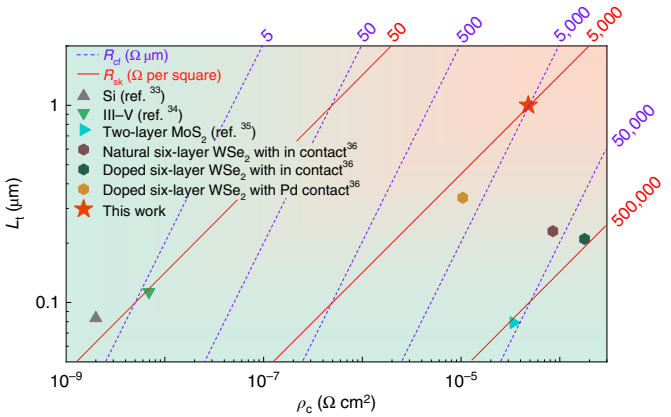

Fig. 5 | Comparison of contact characteristics. L_t is plotted as a function of ρ_c, with contours of constant R_{cf} and R_{sk}. The R_{cf} contour assumes a contact length much longer than L_t. Results for this work are shown for $V_{gs} = -100$ V.

This study shows that R_c can be substantially reduced for TMDs by avoiding damage or strain in the TMD layer. Notably, although bulk semiconductor contacts show transfer length approximately equal to the thickness of the diffused semiconductor sheet[25], the contacts studied here have a transfer length of 1 μm, approximately three orders of magnitude larger than the thickness. The low-resistance contacts demonstrated here will be of immediate application for micrometre-scale devices, for instance, in optoelectronic applications and fundamental studies of TMD physics. Deep scaling of TMD-based FETs, on the other hand, will require much lower values of both R_c and L_t. Simultaneous improvements in both will require large reduction in ρ_c, highlighting the need for research into strategies to improve the coupling between metals and TMDs.

Conclusions

We have reported a strain- and doping-free method to create metal contacts to hBN-encapsulated TMDs. The lack of doping, strain and

damage to the underlying TMD should make it an ideal platform for comparison of theory with experiment. Pt contacts to ultrapure monolayer WSe_2 fabricated using our method exhibit low resistances of 5 kΩ μm and transfer lengths of 1 μm. Our work also highlights that complete characterization—that is, measurement of both R_c and L_t—is crucial for a full understanding of contacts to TMDs. Though a high-work-function metal (Pt) was used here to create a p-type contact, the lack of doping means that this approach could also be used to achieve robust n-type contacts by using low-work-function metals[36,37] (which may require ultrahigh-vacuum assembly), as well as the creation of complementary circuits by combining different metals[36,37]. The platform might also be applied in combination with the hundreds of other high-purity 2D semiconductors[38] to simultaneously achieve low contact resistance and high mobility.

Methods

Cleaving of monolayer WSe_2 and hBN. Flux-grown WSe_2 crystals and hBN bulk crystals were mechanically exfoliated with Scotch tape. Monolayer WSe_2 and thick hBN (tens of nanometres) were cleaved on 285 nm SiO_2 thermally grown on standard four-inch Si wafers. Oxidized silicon was treated in oxygen plasma for 3 min, and the prepared 2D-material-loaded tape was immediately laminated on the fresh silicon oxide surface. The tape was subsequently released from the surface after heating on a hot plate at 100 °C for 3 min. For a thick hBN, we ignored the heating process to consequently achieve a clean surface and easy popping up during the pick-up process.

Preparation of glass slide and stacking. PDMS was prepared from SYLGARD 184 by mixing ten parts base and one part curing agent. Half of the ready-viscous PDMS was embedded into a spare gap of 1 mm between two slices of well-polished silicon wafer and cured at 120 °C for three days to achieve ultrasmooth and ultrahard PDMS elastomer. The other part of PDMS was poured into a plastic Petri dish and cured at 60 °C for 6 h. The second recipe produced a highly elastic PDMS elastomer. To create a glass slide for transferring hBN-embedded three-dimensional (3D) metal electrodes (Supplementary Fig. 2b), we first cut the ultrahard PDMS into a 1 cm × 1 cm square and then mounted it onto a plasma-treated glass slide and heated at 180 °C for 10 min to enhance its adhesion on the glass slide. For the slide (Supplementary Fig. 2a) used for the layer-by-layer pick up, we patterned the soft PDMS into a 0.5 mm × 0.5 mm cube. After gently transferring it onto a glass slide, a layer of clear tape was coated on top and tightened to impose the top surface with a larger curvature used to finely control the individual layer-by-layer pick up. The polypropylene carbonate (PPC) layer was spun on top of a bare silicon wafer, released with a hollow-shaped Scotch tape and then transferred on top of the second type of the glass slide. The final PDMS/PPC block was mounted on a glass slide and heated at 100 °C for 3 min to flatten the top surface. After picking up the hBN and monolayer WSe_2 in a layer-by-layer manner, we released the PPC film, flipped it onto a silicon substrate and loaded it into a high-vacuum annealing furnace to remove the buried PPC at 230 °C for half an hour.

Release of 3D metal electrode–hBN heterostructure. The substrate carrying the hBN-embedded 3D metal electrodes was first decorated in hexamethyldisilazane gas at 180 °C for 20 min. We spin coated bilayer 950 A9 PMMA on top of the decorated substrate. The entire stack underlying the PMMA could be mechanically released from the sacrificial substrate. Then, we gently stacked the PMMA layer on top of the first kind of PDMS glass slide, which could be laminated onto the target substrate (containing monolayer WSe_2/hBN heterostructure). When the polymer conforms uniformly to the substrate, we lifted the slide to disengage the PDMS from the substrate after heating at 80 °C for 30 min. The higher release temperature led to less time needed for disengaging. However, once approaching the glass-transition temperature, undesired strain and stress appear, leading us to make a trade-off.

Raman spectroscopy and AFM. Raman spectra were taken with a Renishaw Raman system using a 532 nm laser source with a power of 1 mW and 10 s duration exposure. The AFM scans were performed using a Bruker AFM instrument in the non-contact mode. Both Raman and AFM characterizations were carried out at room temperature in ambient conditions.

Device fabrication and electrical measurements. Here CHF_3:O_2 (40:4 s.c.c.m.) gas mixture with 60 W radio-frequency power and 40 mtorr gas pressure was used to etch out the hBN in an Oxford Plasmalab 100 inductively coupled plasma–reactive ion etching instrument. The PMMA mask was first patterned on top of the hBN slits using conventional electron-beam lithography, followed by electron-beam metal deposition of Pt/Au (20/80 nm) and a typical lift-off process. The electrical measurements were conducted in a vacuum probe station at room temperature using either a semiconductor parameter analyser (Keysight B1500A) or a Keithley 2400 source meter combined with an SR830 lock-in amplifier.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding authors upon reasonable request.

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Author contributions

Y.L. conceived, led and was involved in all aspects of the project and performed all the design, fabrication, measurement, simulation and data analysis. S.L. grew the WSe_2 crystals and performed the scanning tunnelling microscopy characterizations of the bulk WSe_2 crystals. Z.W. performed the control experiments with evaporated contacts. K.W. and T.T. grew the hBN crystals. W.J.Y. and J.H. advised on the project. Y.L. and J.H. discussed the results and co-wrote the manuscript with input from all the authors.

Competing interests

The authors declare no competing interests.

Additional information

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