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Self-Forming p–n Junction Diode Realized with WSe_2 Surface and Edge Dual Contacts

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Owing to their practical applications, two-dimensional semiconductor p–n diodes have attracted enormous attention. Over the past decade, various methods, such as chemical doping, heterojunction structures, and metallization using metals with different work functions, have been reported for fabrication of such devices. In this study, a lateral p–n junction diode is formed in tungsten diselenide (WSe_2) using a combination of edge and surface contacts. The appearance of amorphous tungsten oxide at etched WSe_2, and the formation of a junction near the edge contact, are verified by high-resolution transmission electron microscopy. The device demonstrates high on/off ratio for both the edge and surface contacts, with respective values of 10^7 and 10^8. The diode can achieve extremely high mobility of up to 168 $cm^2\ V^{-1}\ s^{-1}$ and a rectification ratio of 10^3. The ideality factor is 1.11 at a back gate voltage V_G = 60 V at 300 K. The devices with encapsulation of hexagonal boron nitride exhibit good stability to atmospheric exposure, over a measured period of 2 months. In addition, the architecture of the contacts, which is based on a single-channel device, should be advantageous for the implementation of more complicated applications such as inverters, photodetectors, and light-emitting diodes.

1. Introduction

Owing to the growing need to address scaling problems in electronics, transition metal dichalcogenides (TMDs) have been considered as next-generation semiconductor materials with appropriate bandgap, inherent mobility, and optically ultralow thickness.[1–6] Despite the popularity of conventional Si-based, complementary metal-oxide-semiconductor (CMOS) circuits, ultrathin TMD layers are promising channel replacements because they facilitate structural flexibility and miniaturization for the development of next-generation transparent electronics.[7,8] Among the TMDs, tungsten diselenide (WSe_2), whose monolayer consists of one layer of W atoms sandwiched between two layers of Se atoms, exhibits excellent properties and outstanding potential for use in applications such as valley-based electronics,[9,10] spin-electronics,[11,12] and optoelectronics.[13,14]

Recently, tremendous efforts have been made to build homogeneous TMD materials-based diode devices.[15–17] Several methods to modulate the polarity of TMD devices have been reported, including the use of a high work function interlayer,[18] ionic gating,[19] chemical doping,[20] and dual-channel field-effect transistors (FETs).[16,21] However, the fabricated devices still show poor control of carrier polarity (to either n-type or p-type), regardless of the original work function of the metals used. Most notably, Fermi-level pinning restricts the ability to control polarity by contact engineering, presenting the main obstacle to achieving diode functionality.

In this article, we present a novel strategy to fabricate WSe_2 p–n junction diodes by contact engineering. The combined use of edge and surface contacts to form a p–n junction diode in a single channel of WSe_2 allows us to avoid thickness variations,

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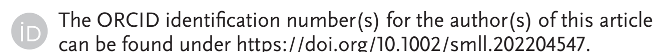
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/smll.202204547.

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DOI: 10.1002/smll.202204547

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which can affect the electrical properties of such diodes.[19,22] This method reduces the number of required fabrication steps, minimizing contamination during the processing. As such, our approach represents a superior contact engineering technique for the fabrication of WSe_2 transistors. Hole characteristics are known to be favored when using edge contacts,[23,24] while the surface contacts lead to n-type behavior, allowing us to realize a WSe_2 homostructure-rectifying diode. The developed diode shows a good ideality factor of 1.11 in the limit of strong induced hole conduction, and the current rectification ratio reaches a value 10^3 without a gate voltage at room temperature. A previous study pointed out that low work function metals are preferable to reduce the Schottky barrier heights (SBHs) in n-type WSe_2.[25] Hence, we selected indium (In) as the surface contact metal because of its appropriate work function (Φ_{In} = 4.12 eV) and it forms a high-quality interface with WSe_2.[26,27] For the WSe_2 edge contact, an amorphous tungsten oxide (WO_x) layer was formed at the etched WSe_2, leading to p-type characteristics in the diode. The electrical behavior and charge transport of each type of contact could be established by extracting the SBH, mobility, contact resistance, and tunneling barrier parameter at different temperatures.

2. Results and Discussion

The fabrication process of the WSe_2 diodes is presented in **Figure 1**a. First, WSe_2 and hexagonal boron nitride (h-BN) flakes (<50 nm thick) were mechanically exfoliated using the Scotch-tape technique. Few-layer WSe_2 (<10 nm thick), chosen by optical contrast before the experiment, was then transferred onto a sacrificial silicon (back-gate) wafer covered by 285 nm SiO_2 (Raman spectra of the WSe_2 flake are shown in Figure S1, Supporting Information). Subsequently, the WSe_2 flake was collected and transferred to the targeted bottom h-BN layer using the dry transfer method.[28] The device pattern was designed

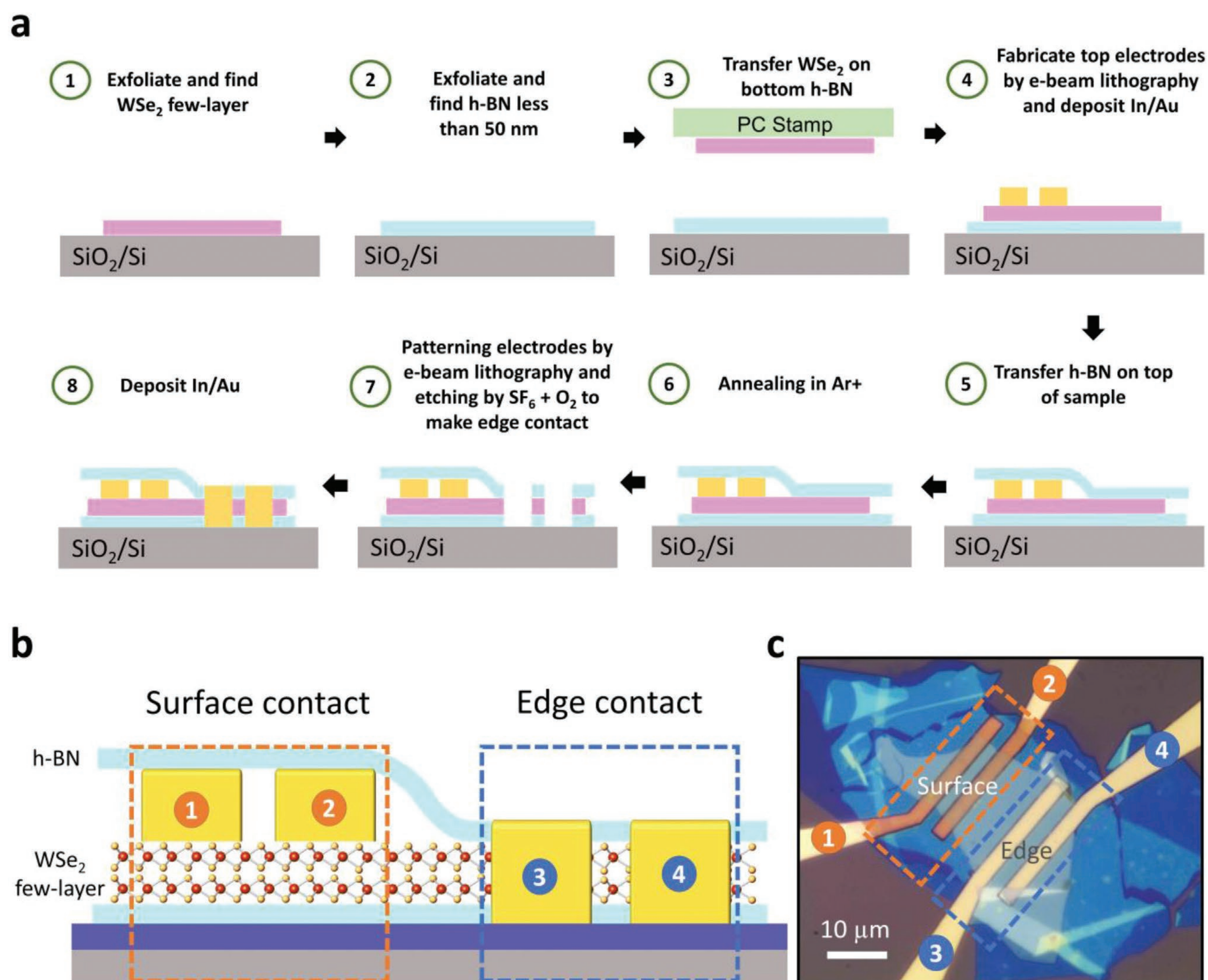

Figure 1. Device process steps and structure. a) Fabrication steps of a WSe_2 p–n diode consisting of h-BN encapsulation with surface and edge contacts. b) Cross-sectional schematic of a WSe_2 p–n diode device. c) Optical microscopy image of the device with each numbered contact. Electrodes 1 and 2 are surface contacts, electrodes 3 and 4 are edge contacts.

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by standard electron-beam lithography (EBL), following which an electron-beam evaporator (pumped to 1×10^{-6} mTorr) was used to deposit the surface contacts [In (10 nm)/Au (30 nm)]. Next, the selected top h-BN flake was taken and stacked on the WSe_2/h-BN bilayer, providing protection for the WSe_2 layer during the fabrication of the edge contacts. The sample was annealed at 150 °C in Argon gas for 2 h to remove bubbles and polymer residues, introduced during the transfer process. Edge contacts were created by using EBL to define the pattern of these electrodes, and by exposing the edges of the WSe_2 by etching in an inductively coupled plasma (ICP, at a pressure of 30 mTorr and power of 30 W) formed from a mixture of oxygen (O_2) (10/30 sccm) and sulfur hexafluoride (SF_6) with an etching time of 100 s. Finally, contact metal was deposited on the exposed edges of the WSe_2. A cross-sectional schematic of the device is presented in Figure 1b, while in Figure 1c we show an optical image of one of the fabricated diodes.

Before measuring the electrical characteristics of the diode device, it is important to separately characterize the carrier type of the surface- and edge-contacted components. The surface-contact properties were measured between contacts 1 and 2, while the electrical performance obtained between electrodes 3 and 4 represented the edge contact behavior (see Figure 1b). Diode performance was then achieved by measuring the electrical properties between electrodes 2 and 3. Thus, three device configurations can be realized, namely, 1–2, 2–3, and 3–4 from left to right, as illustrated in Figure 1c. **Figure 2** shows the electrical performance of the three device configurations. The transfer characteristics of the device were recorded by sweeping the gate voltage in the range of –60 to 60 V, while applying different drain voltages and measuring the resulting drain current at room temperature. The transfer curves of the device demonstrated a typical n-type-dominated behavior WSe_2 for the surface contacts (1–2), with a high current on/off ratio of $\approx 10^8$ and a maximum on current of 25 μA μm^{-1} at V_G = 60 V (Figure 2a). The output curves measured with the In surface contacts exhibited quasi-ohmic behavior that is typically observed with In surface contacts (Figure S3a, Supporting Information). In contrast,

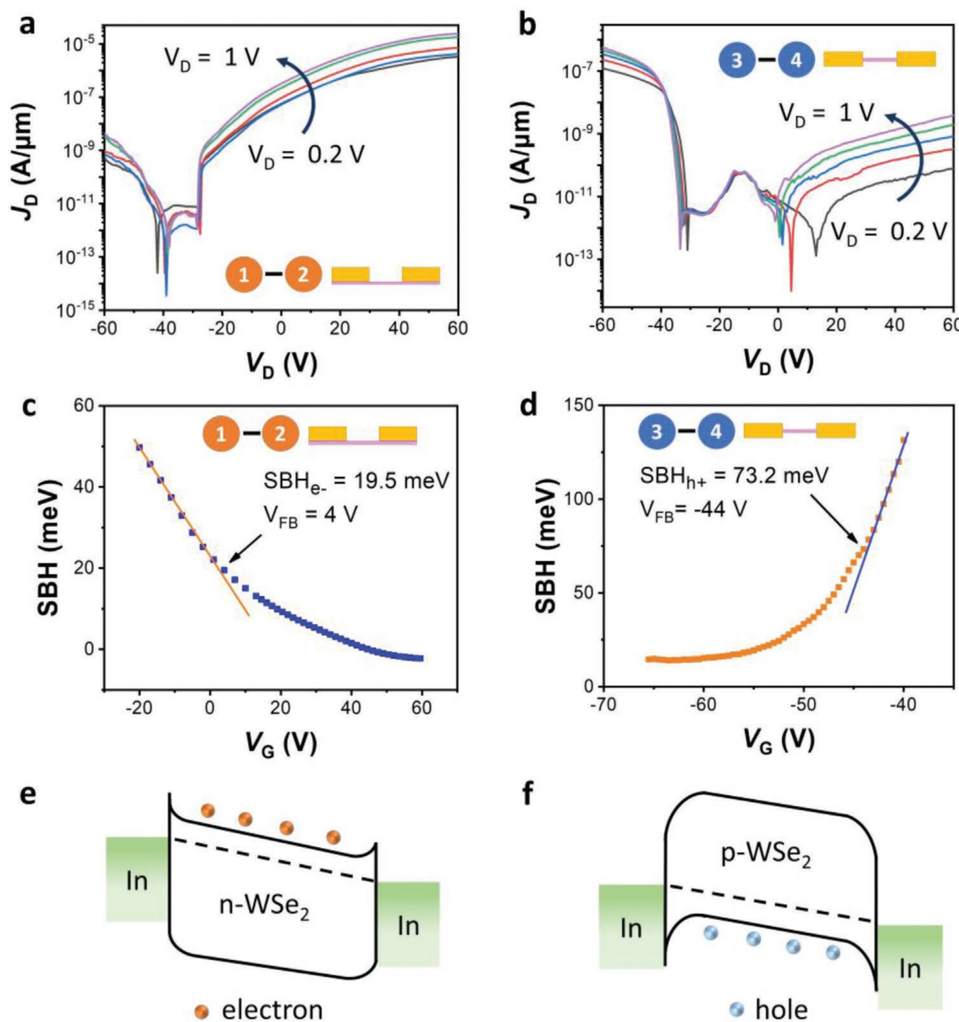

Figure 2. SBH of surface and edge contacts. a,b) The transport characteristic I_D–V_G of the surface and edge contacts with channel width normalization were measured by sweeping gate voltage at various drain voltages from V_D = 0.2 to 1 V at 300 K. c,d) SBH and flat-band voltage of the surface and edge contacts, respectively, determined from the linear slope of the data as a function of gate voltage. e,f) Band alignment of the n-WSe_2 and p-WSe_2 after contact formation with In.

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an unconventional conduction behavior was observed with the edge-contacted device (3–4), as illustrated in Figure 2b. This configuration exhibited p-type polarity even though a low work function metal such as In was used, which reveals the influence of Fermi-level pinning of the edge-contacted WSe_2.[29] These results are consistent with those of Ngo et al., who showed that p-type behavior is always achieved regardless of the work function of the metal used for the metal–semiconductor (MS) contact.[24] The mobility and contact resistance at various temperatures were extracted and are shown in Figure S5 (Supporting Information). The mobility decreased in both surface and edge contacts. This phenomenon demonstrates a dominant influence of phonon scattering on electrical transport rather than impurity scattering.[30–32] The highest mobility was 168 $cm^2\ V^{-1}\ s^{-1}$ was achieved at 77 K for the surface contact. In contrast, the contact resistance increased with temperature (Figure S3d, Supporting Information), indicating that carrier injection from the contacts is dominated more by tunneling than by thermionic emission.[33]

To quantitatively examine the Fermi-level pinning effect of WO_x at the MS interface of the edge contact, temperature-dependent transfer curves were obtained (Figure S4a,b, Supporting Information). These allowed us to extract the SBHs of the surface- and edge-contacted WSe_2 devices. The resulting Arrhenius graphs were studied and used to extract the SBH, $\varnothing_B$, as presented in Figure S4c,d (Supporting Information). For a Schottky-barrier device, current in the subthreshold region arises mostly from thermionic emission and thermally assisted tunneling.[34–36] Following the thermionic emission theory, this current can be expressed as follows:

$$I_D = AA^* T^{3/2} \exp\left(-\frac{q\varnothing_B}{k_B T}\right)\exp\left(\frac{eV_D}{k_B T}-1\right) \tag{1}$$

where I_D is the drain current, A is the cross-sectional area of the device, A^* is the two-dimensional (2D) equivalent Richardson constant, $\varnothing_B$ is the SBH obtained at the flat-band condition (V_{FB}), V_D is the drain voltage, q is the carrier charge, k_B is the Boltzmann constant, and T is the temperature.[35–37] To calculate the SBH, electrical properties were characterized at different temperatures (77–330 K). At $V_{GS} < V_{FB}$, the thermionic-emission current is dominant, while at $V_{GS} > V_{FB}$, the thermally assisted tunneling current becomes substantial and includes other components not accounted for in the thermal emission theory, leading to nonlinear behavior. When $V_{GS} = V_{FB}$, $\varnothing_B$ can be accurately determined as the thermally assisted tunneling does not contribute to the current.[38] The value of $\varnothing_B$ (shown in Figure 2c,d) for the surface and edge contacts is $\varnothing_B$ for holes and electrons, respectively. In this work, the obtained value of $\varnothing_B$ for holes was 73.2 meV at $V_{FB} = -44$ V and $\varnothing_B$ for electrons was 19.5 meV at $V_{FB} = 4$ V. Compared with this, the $\varnothing_B$ value of the edge contacts was approximately four times higher than that of the surface contacts. Based on the extracted SBH, the band structure representing the carrier type of each type of device was plotted, as shown in Figure 2e,f.

To understand the operation mechanism of each component of the p–n diode, cross-sectional high-resolution transmission electron microscopy (HRTEM) was performed to investigate the nature of the MS interface, as demonstrated in **Figure 3**a,b. For both types of contact, the images show an ultraclean surface between h-BN and WSe_2 and a clear crystalline-layered structure, confirming the high-quality stacking of 2D materials realized in this study. In Figure 3a, for the surface contact, the WSe_2 layer underneath the metal shows no significant damage or defects. This implies that an ultrasmooth surface was formed by In, owing to its low melting point, and that a van der Waals gap was induced between the In and the 2D materials.[22,26] Thus, the high performance of the In surface contact was well fitted with the MS interface, as revealed by the energy-dispersive X-ray spectroscopy (EDS) mapping. For the edge-contacted device (Figure 3b), a distinctive contrast to the MS interface was observed for both the surface and edge contacts. The formation of a thick amorphous WO_x layer was observed at the edge of WSe_2 for the latter contact type. This observation was further confirmed by the EDS-mapping spectra illustrated in Figure S2 (Supporting Information). The mechanism for formation of the WO_x layer during the edge-contact fabrication process has been explained by Ngo et al.[24] The thickness of WO_x layer may affect the tunneling current of the edge contact. With the increasing in the WO_x thickness, tunneling resistance will increase leading to the degradation in contact resistance.[39] However, accurately controlling of WO_x formation during edge contact process is

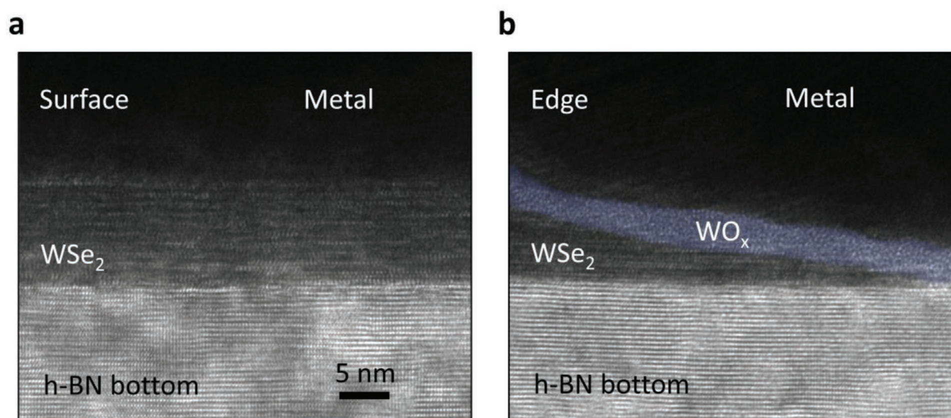

Figure 3. HRTEM of each type of contact. a) Cross-sectional image of the surface contact. b) False-color HRTEM image of the edge contact with the WO_x layer indicated by light, sky-blue region.

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still lack in our research. Thus, it is a potential direction for future research. The presence of the WO_x at the MS interface contributed to the p-type polarity of the WSe_2 edge-contacted device. The highest current in the edge-contacted device was 11 µA, which was obtained at a gate voltage V_G = −60 V with a current on/off ratio of approximately 10^7. Compared with the surface contact, the on current of the edge contact was approximately 40 times lower. The lower current of the edge-contacted device can be attributed to the existence of WO_x layer at MS interface, leading to higher tunneling resistance of the contact.

To further understand the transport characteristics of edge- and surface-contacted WSe_2 in the temperature range of 77–330 K, the Fowler–Nordheim (F–N) tunneling and direct tunneling (DT) models were used. The F–N tunneling and DT mechanism are described by the following equations:[40,41]

Direct tunneling:

$$\ln\left(\frac{I_D}{V_D^2}\right) \propto \ln\left(\frac{1}{V_D}\right) - \left[\frac{4\pi d\sqrt{2m^* \varnothing_B}}{h}\right] \quad (2)$$

Fowler–Nordheim tunneling:

$$\ln\left(\frac{I_D}{V_D^2}\right) \propto -\frac{1}{V_D}\left[\frac{8\pi d\sqrt{2m^* \varnothing_B^3}}{3hq}\right] \quad (3)$$

where $\varnothing_B$ is the tunneling barrier height, m is the free electron mass, m^* (0.34 m) is the effective mass of the electrons in the WSe_2 flake, d is the barrier width, h is the Planck constant, and q is the carrier charge. When $\ln(I_D/V_D^2)$ is plotted as a function of $1/V_D$, all of the curves (at different temperatures) show a logarithmic dependence, indicating that DT is dominant in the device as presented in **Figure 4**a,b. No sign of F–N tunneling was observed for either edge or surface contacts, as reported in several other studies.[20,24,29] Moreover, the tunneling barrier height shown in Figure S6a (Supporting Information) was calculated. The DT barrier parameter $d\sqrt{\varnothing_B}$ could be extracted from the slope of the $\ln(I_D/V_D^2)$ versus $\ln(1/V_D)$ graph. The barrier parameter of the surface contact varied from 0.115 to 0.133 $meV^{-1/2}$ nm when the temperature decreased from 330 to 77 K. The barrier parameter of the edge contact was in the range of 0.164–0.177 $meV^{-1/2}$ nm, when the temperature decreased from 330 to 77 K. It was higher than that of the surface contact because of the presence of the WO_x layer in the edge contact.

Rectifying behavior associated with the presence of a back-to-back diode structure was obtained in the p–n region as shown in **Figure 5**a. This confirmed the intrinsic charge transport of WSe_2 after fabricating the device. To evaluate the rectifying performance of the diode with different contact engineering, the ideality factor was obtained in the forward-biased region from a semilogarithmic plot of the output I–V characteristics, and its fit to the Shockley diode equation.[42]

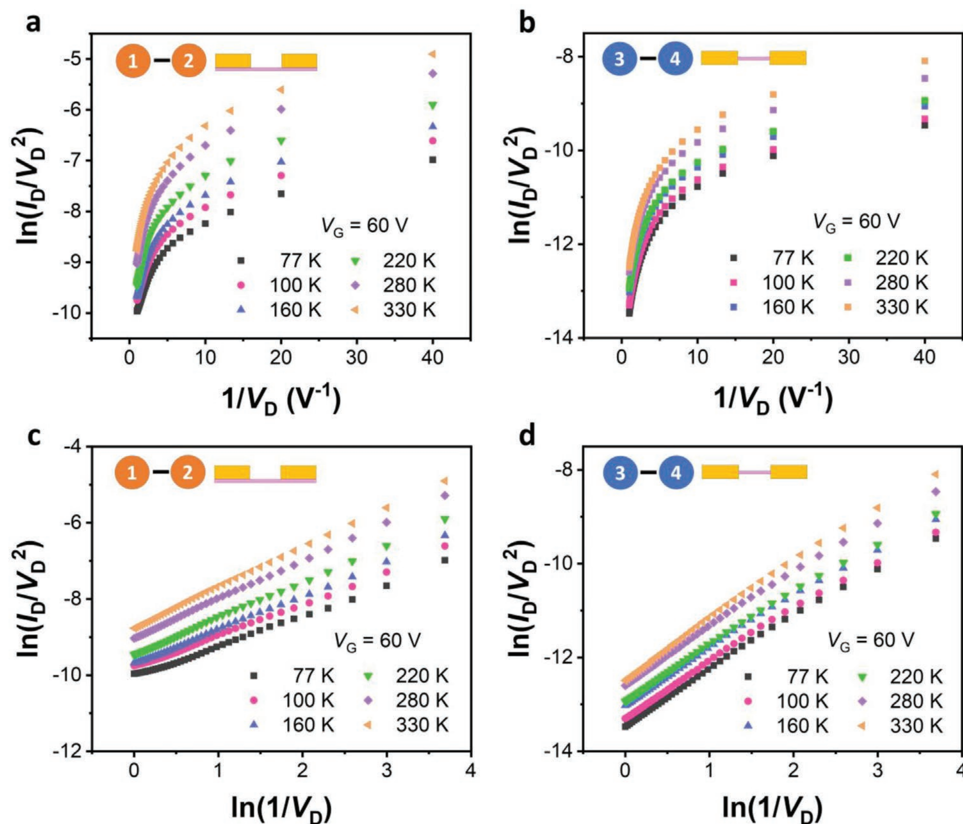

Figure 4. Tunneling behavior of the surface and edge contacts. a,b) $\ln(I_D/V_D^2)$ is plotted as a function of $1/V_D$ at V_G = 60 V for different temperatures. c,d) Graphs of $\ln(I_D/V_D^2)$ versus $\ln(1/V_D)$ at different temperatures and V_G = 60 V showing the linear relation between the DT of the surface and edge contacts. The dashed lines indicate the linear fitting of the DT data.

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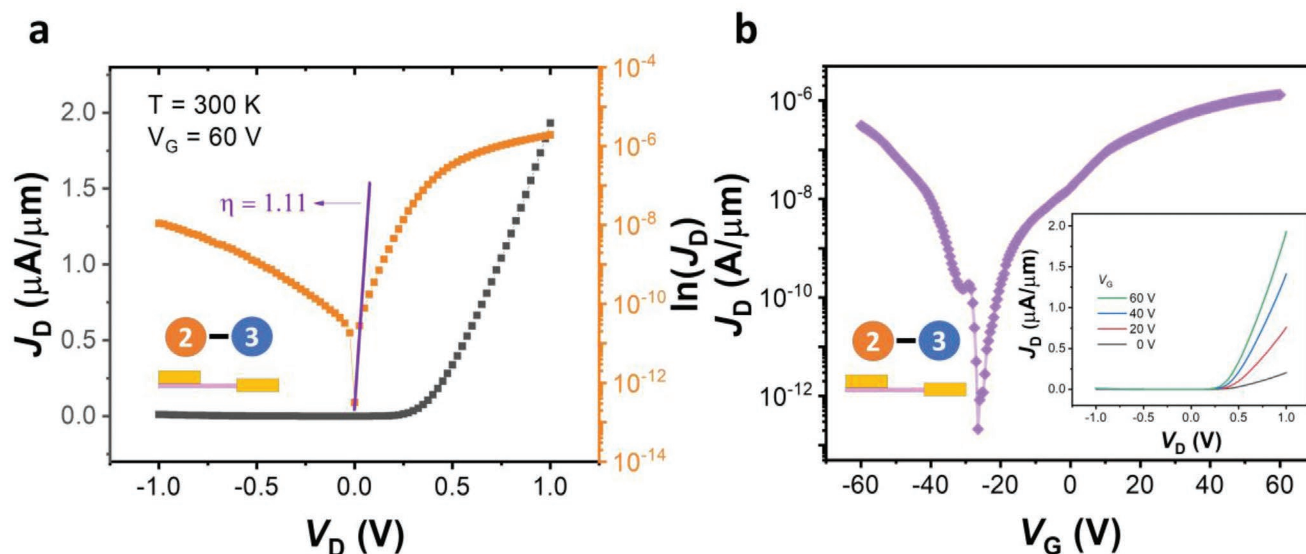

Figure 5. Transfer characteristics of the WSe_2 p–n diode. a) Output characteristics and the ideality factor of the WSe_2 p–n diode, extracted at room temperature from the slope at the low bias region (V_G = 60 V). b) The transfer curve of the diode at room temperature. The inset represents the output curves of the diode for different gate voltages.

$$I = I_S\left[\exp\left(\frac{eV_D}{\eta k_B T} - 1\right)\right] \quad (4)$$

where I is the current of the diode, and I_S the reverse saturation current calculated as follows:

$$I_S = AA^* T^2 \exp\left(-\frac{e\varnothing_B}{k_B T}\right) \quad (5)$$

Here, V_D is the drain voltage, e is the carrier charge, k_B is the Boltzmann constant, T is the temperature in K, η is the ideality factor, A is the diode area, and $A^* = 4\pi q m^* k^2/h^3$ (m^* = 0.34 m_0) is the effective Richardson constant.[10] To calculate the ideality factor η, take the logarithm of both sides and simplify the Shockley diode equation as follows:

$$\eta = \frac{e}{k_B T\left\{\frac{d(\ln I)}{dV}\right\}} \quad (6)$$

Figure 5a shows the logarithm of the I_D–V_D output curves at 300 K. The ideality factor of 1.11 was extracted from the slope of the logarithm I_D–V_D curve at V_G = 60 V. Figure 5b shows the transfer characteristics of the p–n diode, measured in the gate voltage range V_G = –60 to 60 V when applying the drain voltage V_D = 1 V. The inset of Figure 5b shows a typical output curve of the WSe_2 FET. At V_G = 0, the ratio of the forward to the reverse bias current was 10^3 at 300 K, showing the highest rectification ratio among all temperatures (Figure S6, Supporting Information).

By controlling the device polarity using contact engineering, a complementary inverter can be formed by combining n-type and p-type FETs. Generally, the n-type FET is grounded (electrode 1) and the supply voltage (V_{dd}) is applied to the p-type FET (electrode 4). Both the p-type and n-type FETs are controlled by the common back gate that operates as the input voltage (V_{IN}). The output voltage (V_{OUT}) is measured by connecting the n-type and p-type electrodes (electrodes 2 and 3). The CMOS inverter configuration is demonstrated in **Figure 6**b with a logic circuit illustration. The transfer characteristics of the N-MOSFET and P-MOSFET are shown in Figure S3 (Supporting Information), which demonstrates consistent polarity controllability depending on the approaching contacts used. Figure 6c displays the transfer characteristic of the inverter as a function of the V_{IN} with V_{dd} in the range of 3 to 4.5 V, in which a sharp voltage transition is perceived with varying input voltage. The voltage gain achieved a maximum of 1.2 at V_{dd} = 4.5 V (Figure 4d) defined as gain = d_{VOUT}/d_{VIN}. This gain can be further improved by utilization of high-k dielectric, indicating the potential application of WSe_2 CMOS.

3. Conclusions

In summary, a 2D WSe_2 diode was developed through a contact engineering technique that utilized In surface contacts to realize n-type conduction and 1D In edge contacts to achieve p-type behavior. The devices showed excellent performance such as a high on/off current ratio, high mobility, and large rectification ratio. In addition, a WSe_2 CMOS logic inverter was demonstrated for applications. As such, this work provides a novel method for controlling the device polarity of 2D WSe_2 by contact engineering. Significantly, the devices showed good stability performance for 2 months owing to the h-BN encapsulation technique. This method is expected to be applicable to other 2D materials, something that should be the study of further research.

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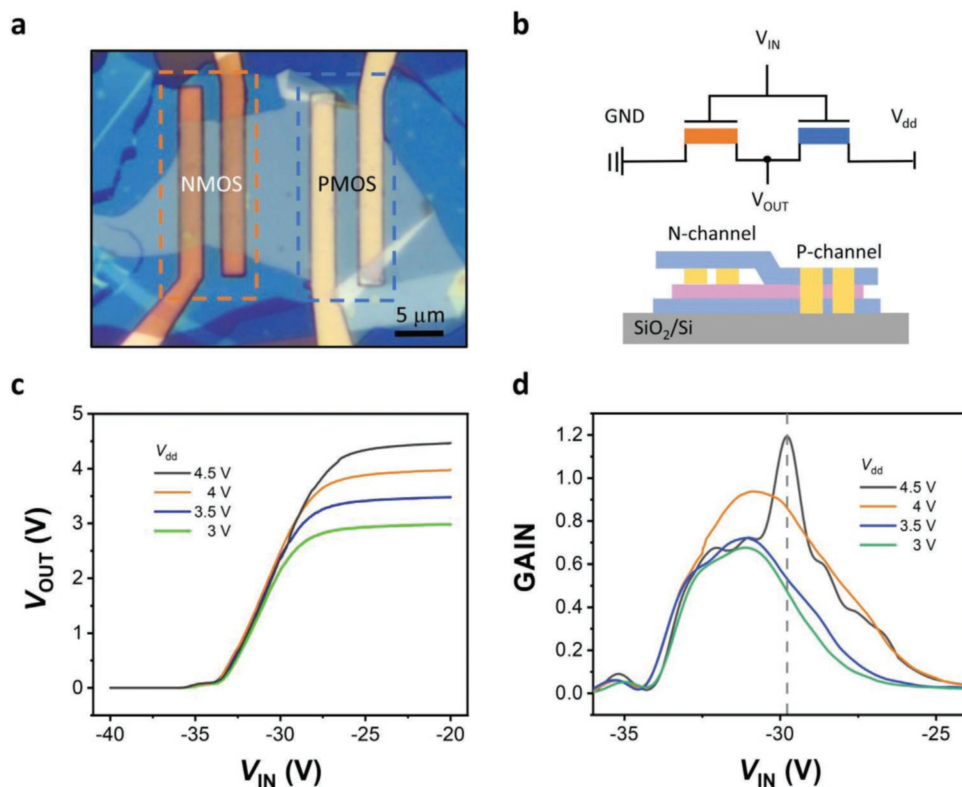

Figure 6. Inverter based on complementary WSe_2 FETs. a) The optical microscope image of the device is marked by the orange and blue dash line boxes for the surface and edge contacts, respectively. b) The schematic image and circuit diagram of the WSe_2-based CMOS inverter with Indium surface contact (N-MOSFET) and Indium edge contact (P-MOSFET). c) The voltage transfer characteristics of the inverter as a function of V_{IN} at various V_{dd}. d) The voltage gain of the WSe_2-based diode inverter as a function of input voltage for various supply voltages.

4. Experimental Section

Fabrication of WSe_2 p–n Diode Device: Bulk n-type WSe_2 crystal (HQ graphene Inc.) was used for exfoliation on the highly p-doped Si substrate covered by a 285 nm-thick SiO_2 layer. Electrodes were patterned using electron-beam lithography and the etching process was performed using an ICP plasma-etching machine with a mixture of SF_6 and O_2. In and Au were deposited by an electron-beam evaporator (Korea Vacuum Tech. KVT-2004).

Characterization of WSe_2 Device: Raman spectroscopy was performed to characterize the thickness of the flake. Electrical characterization of the device was measured under a vacuum condition below 20 mTorr in a dark environment and using a Keithley 4200-SCS parameter analyzer connected to the probe station.

HRTEM and EDS at the Interface of the Metal–Semiconductor: HRTEM image was obtained to observe the cross-sectional of the edge and surface contacts after fabrication. Apart from the HRTEM images, EDS mapping and line scanning were performed to determine the doped elements ingredients in the sample.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT) (grant Nos. 2019R1A2C2088719 and 2021K2A9A2A08000168). K.W. and T.T. acknowledge support from the Elemental Strategy Initiative conducted by the MEXT, Japan, grant No. JPMXP0112101001, JSPS KAKENHI grant Nos. JP20H00354 and the CREST (JPMJCR15F3), JST.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

edge contacts, inverters, p–n diodes, transition metal dichalcogenides, WSe_2

Received: July 23, 2022
Revised: September 8, 2022
Published online: October 10, 2022

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