Solid-State Electronics 54 (2010) 14–17

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

# Pulse-agitated self-convergent programming for 4-bit per cell dual charge storage layer flash memory

Gang Zhang, Won Jong Yoo *

*Sungkyunkwan University, SKKU Advanced Institute of Nano-Technology, 300 Cheoncheon-dong, Jangan-gu Suwon 440-746, Republic of Korea*

ARTICLE INFO

*Article history:*
Received 28 August 2008
Received in revised form 17 July 2009
Accepted 8 September 2009
Available online 9 October 2009

The review of this paper was arranged by Prof. S. Cristoloveanu

*Keywords:*
Pulse-agitated self-convergent programming
4-Bit per cell
DCSL memory

ABSTRACT

A pulse-agitated (PA) self-convergent programming (SCP) scheme is proposed for 4-bit per cell vertically dual charge storage layer (DCSL) Flash memory operation in NOR-circuits. PA substrate hot electron injection (PASHEI) is used for programming, and hot hole injection (HHI) is used for erasing. Localized PASHEI enables separated data nodes, while clear electron energy modulation gives rise to accurate multi-level threshold voltage ($V_{th}$) control in the step-up potential wells of the DCSL devices. Excellent 4-bit cell reliability is maintained for the DCSL devices throughout the $10^5$ programming/erasing (P/E) cycles, and inter-cell disturbances are suppressed.



## 1. Introduction

Recently, Flash memory using a $ZrO_2/Si_3N_4$ DCSL has been proposed for highly-reliable multi-level data storages, and a programming scheme based on Fowler–Nordheim (F–N) tunneling and channel hot electron injection (CHEI) was implemented in the operation of the DCSL devices in NAND-circuit [1]. Nevertheless, the F–N/CHEI scheme brings about complex operations, in which the programming mode has to be selected for different $V_{th}$ levels. i.e., F–N tunneling is designed for levels 01/10, while CHEI is designed for level 00 [1]. Moreover, the high-voltage CHEI operations, i.e., by gate voltage ($V_g$) $\geqslant$ 18 V and drain-to-source voltage ($V_{ds}$) $\geqslant$ 8 V, results in serious bit-line disturbances in NAND-circuits, giving rise to various reliability issues.

In this work, a PA-SCP scheme based on PASHEI programming and HHI erasing is proposed to achieve 4-bit per cell (separated data nodes + multi-level cell) operation for the DCSL devices in NOR-circuit. Pulse voltages are applied to gate and drain (source) for Node-2 (Node-1) programming, and the amplitudes of $V_g$ and $\pm V_{ds}$ ($\pm V_{sd}$) are adjusted to control levels 10/01/00 at the corresponding data node. PASHEI is localized in the channel/drain junction, as shown in Fig. 1 [2,3], thus it prevents the data storage at one data node from being disturbed by the opposite data node until the second-bit effects become intolerable [4,5]. Meanwhile, the separated data storages in the 1st and 2nd-wells of the DCSL structure are immune to their mutual disturbances due to the 2nd-potential barrier control [1]. Moreover, the low-voltage PASHEI, i.e., by $V_g \leqslant 10$ V, $V_{ds} \leqslant 7$ V, has consistent charge injection profiles with HHI, suppressing inter-cell disturbances induced by high voltage operation and endurance degradation induced by channel charge accumulation during the separated data nodes operations [5,6]. By modulating the electron energy ($\varphi_e$) to match the step-up potential wells during PA-SCP [1], 4-bit per cell operation is accomplished for the DCSL devices, in which the 4-bit cell data clearance is maintained throughout the $10^5$ P/E cycles, and inter-cell disturbances are suppressed throughout the entire range of the P/E voltages. Therefore, PA-SCP implemented with the DCSL devices may be one of the promising techniques to achieve highly-reliable 4-bit per cell memory application in near future.

## 2. Mechanism

In the $ZrO_2/Si_3N_4$ DCSL, $ZrO_2$ has a conduction band offset $\Delta\varphi_c$ = 2.1 eV to $SiO_2$ and 1.0 eV to $Si_3N_4$ to form the 1st-well. The tunnel oxide and $ZrO_2/Si_3N_4$ interface perform as the 1st and 2nd-potential barriers, controlling the electron influx and electron distribution, respectively. When $\varphi_e$ is less than 1 eV, the incoming electrons are blocked by the 2nd-barrier, and some of them are trapped in the 1st-well ($ZrO_2$) to enable level 10 programming. When $\varphi_e$ is between 1–3.2 eV, the incoming electrons overcome the 2nd-barrier but are blocked by the block oxide. Some electrons are trapped in the 2nd-well ($Si_3N_4$) to achieve level 01 program-

* Corresponding author. Tel.: +82 31 290 7468; fax: +82 31 299 4119.
*E-mail address:* yoowj@skku.edu (W.J. Yoo).

0038-1101/$ - see front matter © 2009 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2009.09.009

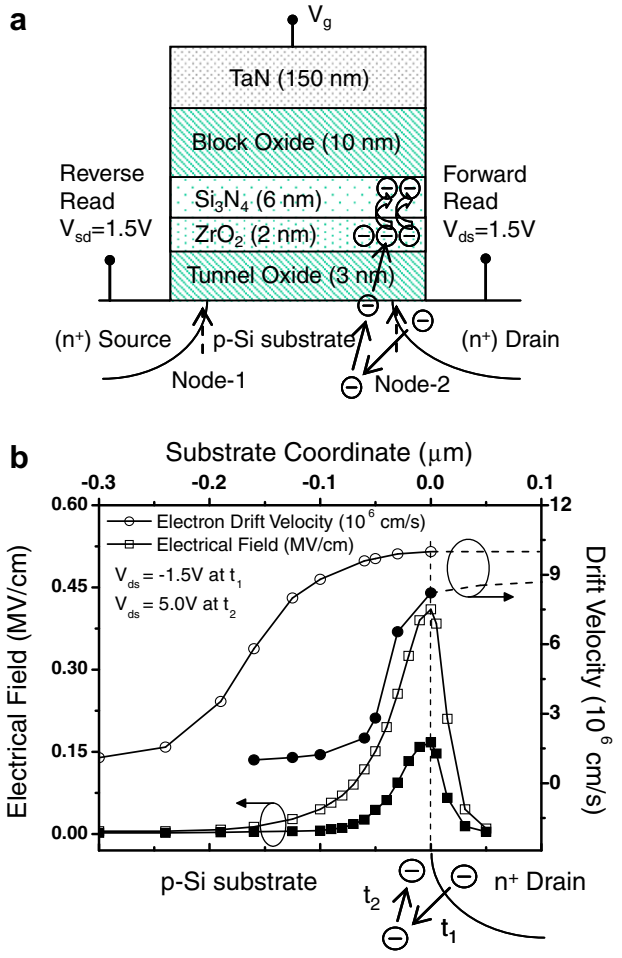


**Fig. 1.** (a) Schematic of the device structure of a $ZrO_2/Si_3N_4$ DCSL memory and the demonstration of pulse-agitated programming. Localized PASHEI enables HE injection/tunneling near the channel/drain junction (Node-2) without disturbing the channel/source region (Node-1) for 2-bit program, and HE energy is modulated to match the step-up potential wells of DCSL to achieve accurate $V_{th}$ control. (b) The estimated $E_{acc}$ over the PN junction, and the corresponding electron drift velocities. (Solid symbols are for forward bias at $t_1$, and open symbols are for reverse bias at $t_2$.)

ming. When $\varphi_e$ is larger than 3.2 eV, the injected electrons overcome the potential difference of $ZrO_2/Si_3N_4$, being confined only into the 3rd-well between the tunnel and block oxides after hot electron relaxation to achieve level 00 programming [1]. Level merge between levels 10/01/00 is prevented by the separated charge storage in the step-up potential wells, giving rise to improved multi-level cell reliability [1].

The mechanisms of PASHEI have been investigated earlier. As shown in Fig. 1a, with grounded substrate and $-V_{ds}$, the PN junction between the p-Si substrate and the $n^+$ drain is forward biased, and the conduction band electrons in $n^+$ drain are accelerated by the electrical field over the PN junction, which is known as the HE emission during the emission pulse $t_1$ [2,3]. The accelerated HEs during $t_1$ will be relaxed promptly and behave as free electrons in the conduction band of the p-Si substrate, since the HE relaxation time is only $10^{-14}$–$10^{-13}$ s [7,8]. For example, the peak of the accelerating field ($E_{acc} \approx 1.5 \times 10^5$ V/cm) is ~0.05 μm from the channel/drain junction when $V_{ds} = -1.5$ V is applied, while $E_{acc}$ decays exponentially to $5 \times 10^4$ V/cm beyond 0.075 μm from the gate/drain junction, as shown in Fig. 1b (solid symbols) [8]. Accordingly, the electron drift velocity sharply decays from $9 \times 10^6$ cm/s at the peak of $E_{acc}$ to ~$1.5 \times 10^6$ cm/s at the p-Si substrate (~0.07 μm from the junction) [8,9]. As a result, the emitted electrons are likely to accumulate near the boundary (0–0.07 μm) of the PN junction due to the sharp decrease of the drift velocities. It is noticed that the electron recombination lifetimes in p-Si substrate are 0.1–2 μs [7]. It is thus understood that the relaxed electrons behave as excess electrons in the conduction band of p-Si substrate before recombination within $t_1$ = 1–2 μs [7,9].

During the accelerating pulse $t_2$ [2,3], the PN junction between the p-Si substrate and the $n^+$ drain is reverse biased by the grounded substrate and $+V_{ds}$. For example, $E_{acc}$ drastically increases from ~$2 \times 10^4$ V/cm to ~$4.5 \times 10^5$ V/cm from ~0.2 μm beyond the channel/drain junction when an accelerating bias of $+V_{ds} = 5$ V is applied, and the electron drift velocity increases from ~$2 \times 10^6$ cm/s to ~$10.5 \times 10^6$ cm/s accordingly, as shown in Fig. 1b (open symbols). As the reverse-biased PN junction acceleration region (0.2 μm) covers the excess electron accumulation region (0–0.07 μm), the excess electrons emitted during $t_1$ can be readily accelerated and guided towards the gate by $+V_g$ and $+V_{ds}$ at $t_2$. Some electrons obtain sufficient energy to be tunneled/injected via the tunnel oxide, enabling the PASHEI programming. In contrast, CHEI occurs only in the inverted channel, being limited by the pinch-off effect and channel HEs scattering [10]. We thus think that the efficiency of PASHEI can be significantly enhanced by the excess electrons compared to that of CHEI [2,10].

According to above analysis, it is understood that accurate $V_{th}$ control can be realized by using PASHEI once if $\varphi_e$ is modulated to match the step-up potential wells of the DCSL devices. On the other hand, it is noticed that the $\varphi_e$ control during PASHEI may be similar to that of CHEI, in which $\varphi_e$ obeys the Boltzmann-Maxwell distribution, while the electron temperature is linearly proportional to $+V_{ds}$ [8,10]. Therefore, by adjusting $+V_{ds}$, $\varphi_e$ may be controlled to accomplish PA-SCP for the DCSL devices.

## 3. Results and discussion

Fig. 2a (inset) shows the 2-bit property for a DCSL device with the gate length $L_g$ = 2 μm. Pulse voltages of $\pm V_{ds} = -2/7$ V, $V_g$ = 10 V are applied for programming, and $V_{ds}$ = 8 V, $V_g = -15$ V are applied for erasing. $10^4$ pulses result in a ~4.7 V window between the reverse and forward read $V_{th}$. PASHEI is understood to be less dependent on the channel electron acceleration but it occurs only in the channel/drain junction, as shown in Fig. 1a, enabling enhanced 2-bit scalability compared to CHEI [2,3]. The second-bit effects were monitored for PA-SCP by using reference devices ($L_g$ = 70–300 nm) [4,5], which have the same structure as the DCSL devices, with only difference in excluding the $ZrO_2$ layer. It is found that the second-bit effects is unavoidable for CHEI when $L_g \leqslant 140$ nm, while they are prevented for PASHEI when $L_g \geqslant 110$ nm [2], as shown in Fig. 2a. This suggests that better scalability can be achieved by using PA-SCP (PASHEI) compared to the other SCP schemes (CHEI) [4–6]. Memory windows of ~4 V are used to attain the reliable data clearance in the 4-bit per cell operation. However, it is found that the second-bit effects are insensitive to the enlarged memory windows, since the PASHEI profiles remain unchanged (~70 nm) for various programming conditions, while the different HE densities may dominate the multi-level control [2].

Fig. 2b shows the multi-level P/E transient characteristics of a DCSL device. With source and substrate grounded, $\pm V_{ds} = -2/5$ V, $-2/6$ V, $-2/7$ V and $V_g$ = 10 V are applied for levels 10/01/00 programming, and $V_{ds}$ = 8 V, $V_g = -15$ V are applied for erasing. When pulse widths $t_1 = t_2$ = 2 μs, ~$10^5$ pulses give saturated $V_{th}$ levels 10, 01 and 00 at 2.30 V, 4.34 V and 6.29 V. Initial $V_{th}$ level of a fresh DCSL cell is used as level 11 at 1.32 V. It is noticed that the HEI ($\varphi_e > 3.2$ eV) density ($N_e$) is too small to trigger effective programming when small $V_{ds}$ is applied for PASHEI, i.e., $N_e < 10^6$ cm$^{-3}$ for

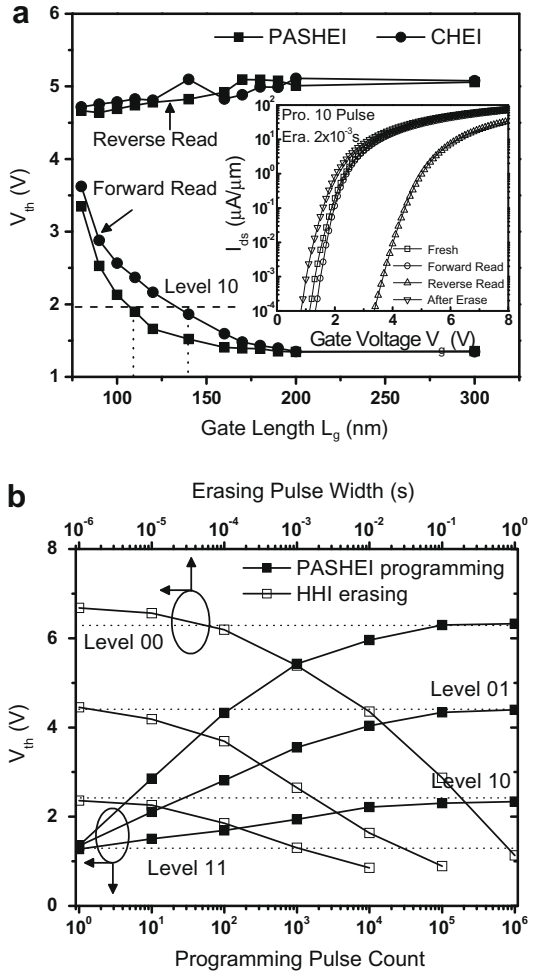


**Fig. 2.** (a) The second-bit effects induced by CHEI and PASHEI at $10^4$ pulses for the reference devices with a gate length $L_g$ = 70–300 nm, and the effects of 2-bit programming for DCSL devices with $L_g$ = 2 μm by PASHEI. Distinct $V_{th}$ levels are attained at Node-2 from forward/reverse read at 10 pulses (inset). (b) Multi-level characteristics by PASHEI programming and HHI erasing for a 2 μm DCSL device at data Node-2. $\pm V_{ds}$ = −2/5 V, −2/6 V, −2/7 V, and $V_g$ = 10 V are applied for levels 10/01/00 programming, and $V_{ds}$ = 8 V, $V_g$ = −15 V are applied for erasing.

$V_{ds} \leqslant 5$ V, and $N_e < 10^9$ cm$^{-3}$ for $V_{ds} \leqslant 6$ V [8]. We thus think that the HE tunneling ($\varphi_e < 3.2$ eV) may dominate the levels 10/01 programming when $V_{ds} \leqslant 6$ V [10]. When $V_{ds}$ = 7–9 V, $N_e > 10^{12} - 10^{13}$ cm$^{-3}$, effective HEI is enabled for level 00 programming [1]. Over-erasure is observed for HHI erasing of levels 10/01/00 due to the large valance band offset of $Si_3N_4$ ($\Delta\varphi_v$ = 2.4 eV) to $SiO_2$ [1]. However, the disturbances induced by over-erasure can be spontaneously corrected by the saturated inner levels 10 and 01. For example, the programmed levels 10 and 01 saturate at ~2.30 V and ~4.34 V, even if the base level is over-erased. As a result, the 4-level clearance can be properly maintained [1]. The sensing windows between levels 11/10/01/00 are larger than 1 V throughout the $10^5$ P/E cycles, in which levels 10 and 01 saturate at 2.26 V and 4.35 V, being immune to various programming disturbances. Level 00 increases from 6.61 V to 7.23 V after $10^5$ P/E cycles, due to high voltage stress induced tunnel oxide degradation [5], and level 11 decreases from 1.32 V to 0.40 V due to HHI induced over-erasure, similar to the reported results in [1]. It is noticed that large $V_{ds}$ (up to 8 V) is applied to long-channel DCSL devices ($L_g$ = 2 μm). However, it is expected that the P/E $V_{ds}$ can be reduced for short-channel devices, i.e., $V_{ds}$ = 5.5 V is applied for CHEI programming for NROM devices with $L_g$ = 190 nm [5], due to higher effective lateral electrical field control. Table 1 lists the PA-SCP scheme and the resulting $V_{th}$ levels.

**Table 1**
Programming scheme and the $V_{th}$ results.

| Node | Level | Program (V) | | $V_{th}$ (V) |
|---|---|---|---|---|
| | | $\pm V_{sd}$ | $V_g$ | $V_{ds}$ = 1.5 V |
| 1 | 11 | 0 | 10 | 1.32 |
| | 10 | −2/5 | 10 | 2.76 |
| | 01 | −2/6 | 10 | 4.32 |
| | 00 | −2/7 | 10 | 6.03 |
| | | $\pm V_{ds}$ | $V_g$ | $V_{sd}$ = 1.5 V |
| 2 | 11 | 0 | 10 | 1.34 |
| | 10 | −2/5 | 10 | 2.65 |
| | 01 | −2/6 | 10 | 4.32 |
| | 00 | −2/7 | 10 | 5.94 |

The $\varphi_e$-dependent vertical charge distribution has been studied for levels 10/01/00. The separation of the charge storages in the 1st-well ($ZrO_2$) for level 10, in the 2nd-well ($Si_3N_4$) for level 01, and in the 3rd-well (bulk $ZrO_2$ and $Si_3N_4$) for level 00 have been confirmed by the consistent results obtained from the transient current experiments and simulation [1]. As $Si_3N_4$ is the main charge trapping medium, the retention properties of the DCSL devices may be explored, similarly to those of 4-bit per cell NROM devices. Moreover, the suppression of over-erasure induced leakage may also be investigated as that for the devices using a $Si_3N_4$ trapping layer [11].

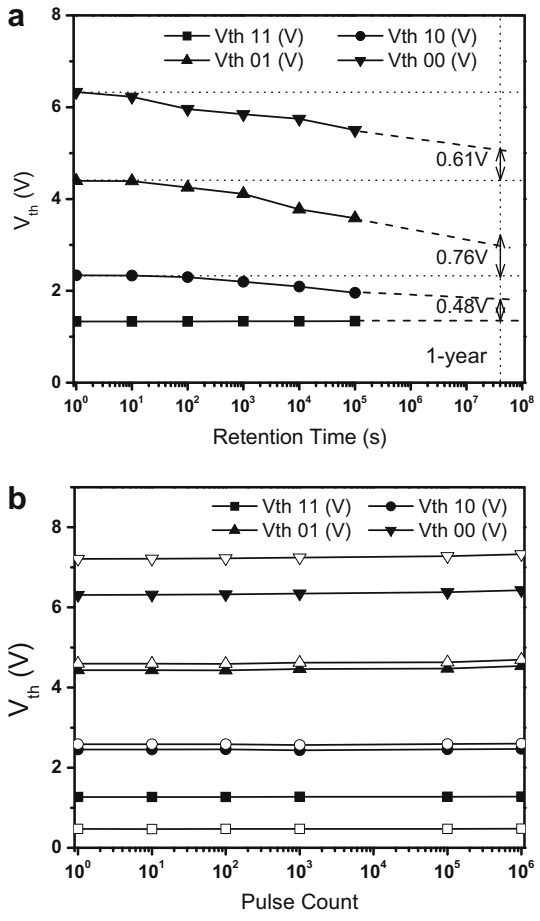


**Fig. 3.** (a) The 4-level charge retention properties at Node-2 at 360 K for the 4-bit per cell DCSL devices with $L_g$ = 2 μm and (b) the effects of drain disturbance at Node-2 when $V_g$ = 0 V, $V_{ds}$ = 7 V are applied for up to 0.2 s (≈$10^5$ P/E cycles). Negligible $V_{th}$ level variations are detected at Node-2. (Solid symbols for fresh devices, and open symbols for devices after $10^5$ P/E cycles.)

Fig. 3a shows the 4-level charge retention properties for Node-2 (reverse-read) of the 4-bit per cell DCSL devices with $L_g = 2$ μm. Clear $V_{th}$ windows are maintained for $3 \times 10^7$ s at 360 K, and the remaining sensing windows are found to be 0.48 V, 0.76 V and 0.61 V between levels 11/10/01/00, respectively. The $V_{th}$ decay for levels 10/01/00 may be due to the trapped electrons discharge and direct tunneling via the thin (3 nm) tunnel oxide [1]. However, no evidences have been proposed for charge retention degradation induced by lateral charge migration for the $Si_3N_4$ based memory devices [4–6]. Fig. 3b shows the effects of gate and drain disturbances from 2-bit and 4-level programming for DCSL devices with $L_g = 2$ μm. $V_g = 10$ V, $V_{sd} = 0$ V are applied to Node-1. The forward read level 11 increases from 1.32 V to 1.62 V by 0.2 s, while the forward read levels 10/01/00 and the reverse read levels 11/10/01/00 remain unchanged for a device and that after $10^5$ P/E cycles, respectively, as reported in [1]. It is understood that F–N tunneling is unavoidable for DCSL devices with a thin (3 nm) tunnel oxide when $V_g \geqslant 9$ V [1]. Thicker oxide, e.g., 5 nm, can effectively suppress such gate disturbances induced by F–N tunneling [2]. On the other hand, when $V_g = 0$ V, $V_{ds} = 7$ V are applied to Node-2, negligible $V_{th}$ level variation is observed throughout the $10^6$ pulses even after $10^5$ P/E cycles. We think that the immunity to the drain disturbances is probably attributed by the low-voltage operation of PA-SCP.

## 4. Conclusion

A low-voltage PA-SCP has been proposed for 4-bit per cell DCSL memory application. Based on the step-up potential wells of the DCSL and clear energy control of PASHEI, PA-SCP enables good data clearances and promising data storage reliability for the DCSL devices in NOR-circuit throughout the $10^5$ P/E cycles.

## References

[1] Zhang G, Hwang WS, Santosh MB, Lee S-H, Cho B-J, Yoo WJ. Novel $ZrO_2/Si_3N_4$ dual charge storage layer to form step-up potential wells for highly reliable multi-level cell application. In: IEDM technical digest, 2007, p. 83–6.
[2] Chung SS, Tseng YH, Lai CS, Hsu YY, Ho E, Chen T, et al. Novel ultra-low voltage and high-speed programming/erasing scheme for SONOS flash memory with excellent data retention. In: IEDM technical digest, 2007, p. 457–60.
[3] Liu Z, and Ma TP. A low voltage erase technique for DINOR flash memory devices. In: VLSI technical digest, 1999, p. 17–8.
[4] Lue H-T, Hsu T-H, Wu M-T, Hsieh K-Y, Liu R, Lu C-Y. Studies of the reverse read method and second-bit effect of 2-bit/cell nitride-trapping device by quasi-two-dimensional model. IEEE Trans Electron Dev 2006;53(1):119–25.
[5] Zhang G, Samanta SK, Singh PK, Ma F-J, Yoo M-T, Roh Y-H, Yoo WJ. Partial crystallization of $HfO_2$ for 2-Bit/4-Level SONOS-type flash memory. IEEE Trans Electron Dev 2007;54(12):3177–85.
[6] Fuks D, Kiv A, Roizin Y, Gutman M, Bibi RA, Maximova T. The nature of HT Vt shift in NROM memory transistor. IEEE Trans Electron Dev 2006;53(2):304–13.
[7] Fahrenbruch AL, Bube RH. Fundamentals of solar cells. Academic Press; 1983.
[8] Toriumi A, Yoshimi M, Iwase M, Akiyama Y, Taniguchi K. A study of photon emission from n-channel MOSFET's. IEEE Trans Electron Dev 1987;ED34(7):1501–8.
[9] Dimitrijev S. Understanding semiconductor devices. New York: Oxford University Press; 2000.
[10] Zhang G, Yoo WJ, Ling CH. Hot-electron capture for CHEI programming in SONOS-type flash memory using high-k trapping layer. IEEE Trans Electron Dev 2008;55(6):1502–10.
[11] Eitan B, Cohen G, Shappir A, Lusky E, Givant A, Janai M, et al. 4-bit per cell NROM reliability. In: IEDM technical digest 2005, p. 539–42.